PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC10 1987

Memories

MOS, TTL, ECL

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MEMORIES MOS, TTL, ECL

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COMPONENTS AND MATERIALS	GREEN

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Instrument tubes, monitor and display tubes, C.R. tubes for special applications

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S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

S14 **Liquid Crystal Displays**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of handbooks comprises:

IC01	**Radio, audio and associated systems** Bipolar, MOS	published 1986
IC02a/b	**Video and associated systems** Bipolar, MOS	published 1986
IC03	**Integrated circuits for telephony** Bipolar, MOS	published 1986
IC04	**HE4000B logic family** CMOS	published 1986
IC05N	**HE4000B logic family — uncased ICs** CMOS	published 1984
IC06N	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	published 1986
IC08	**ECL 10K and 100K logic families**	published 1986
IC09N	**TTL logic series**	published 1986
IC10	**Memories** MOS, TTL, ECL	new issue 1987
IC11N	**Linear LSI**	published 1985
Supplement to IC11N	**Linear LSI**	published 1986
IC12	**I²C-bus compatible ICs**	not yet issued
IC13	**Semi-custom** Programmable Logic Devices (PLD)	new issue 1987
IC14	**Microcontrollers and peripherals** Bipolar, MOS	new issue 1987
IC15	**FAST TTL logic series**	published 1986
IC16	**CMOS integrated circuits for clocks and watches**	published 1986
IC17	**Integrated Services Digital Networks (ISDN)**	not yet issued
IC18	**Microprocessors and peripherals**	new issue 1987

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C6	**Synchronous motors and gearboxes**
C7	**Variable capacitors**
C8	**Variable mains transformers**
C9	**Piezoelectric quartz devices**
C11	**Varistors, thermistors and sensors**
C12	**Potentiometers, encoders and switches**
C13	**Fixed resistors**
C14	**Electrolytic and solid capacitors**
C15	**Ceramic capacitors**
C16	**Permanent magnet materials**
C17	**Stepping motors and associated electronics**
C18	**Direct current motors**
C19	**Piezoelectric ceramics**
C20	**Wire-wound components for TVs and monitors**
C22	**Film capacitors**

SELECTION GUIDE

FUNCTIONAL INDEX

NUMERICAL INDEX

MOS MEMORIES

Introduction

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

The FIRST LETTER divides the solitary circuits into:

S : Solitary digital circuits
T : Analogue circuits
U : Mixed analogue/digital circuits

The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

MA : { Microcomputer / Central processing unit
MB : Slice processor (see note 2)
MD : Correlated memories
ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The FIRST TWO LETTERS identify the following:

NH : Hybrid circuits
NL : Logic circuits
NM : Memories
NS : Analogue signal processing, using switched capacitors
NT : Analogue signal processing, using CTDs
NX : Imaging devices
NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line
W : Lead chip-carrier (LCC)
X : Leadless chip-carrier (LLCC)
Y : Pin grid array (PGA)

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device.

An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

Characteristic

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those charactersistics which are directly related to the application.

Rating

A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

Rating system

The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

CMOS RAM

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and CE2, selection being made when $\overline{CE1}$ is LOW and CE2 is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range 2,5 to 5,5 V
- Low data retention voltage min. 1 V
- Low power consumption in both operating and standby modes
- Access time 150 ns at V_{DD} = 5 V; 400 ns at V_{DD} = 3 V
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

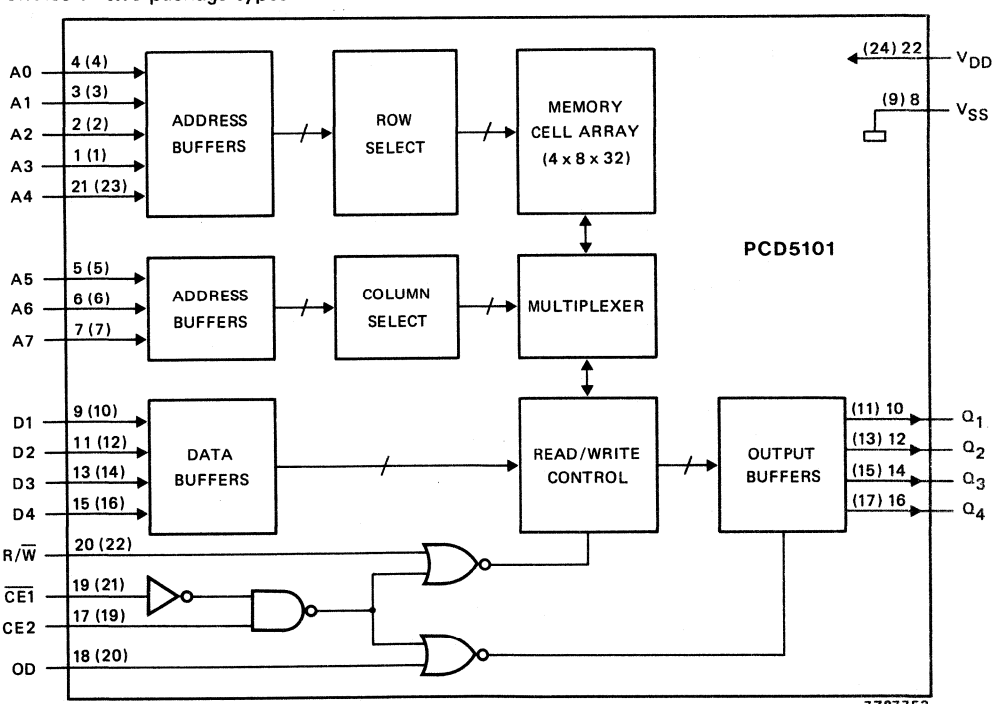


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT-116).
PCD5101T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

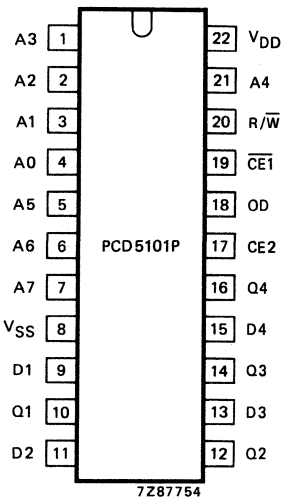


Fig. 2 Pinning diagram for PCD5101P.

PINNING

D1 D2 D3 D4	data inputs
A0 A1 A2 A3 A4 A5 A6 A7	address inputs
R/$\overline{W}$	read/write input
$\overline{CE1}$ CE2	chip enable inputs
OD	output disable
Q1 Q2 Q3 Q4	data outputs
V_{DD}	positive supply
V_{SS}	negative supply
n.c.	not connected

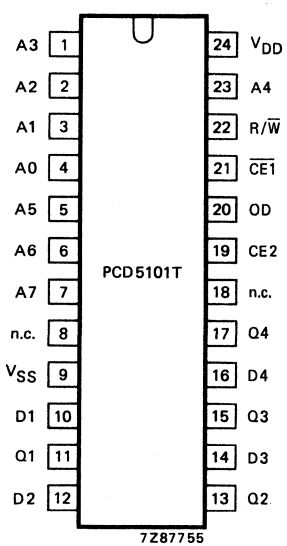


Fig. 3 Pinning diagram for PCD5101T.

OPERATING MODES

Table 1 Mode selection

$\overline{CE1}$	CE2	R/$\overline{W}$	OD	mode of operation	output state
H	X	X	X	standby	high impedance
X	L	X	X	standby	high impedance
L	H	L	H	write	high impedance
L	H	L	L	write	equal to input data
L	H	H	L	read	data valid
L	H	H	H	read	high impedance

Separate input/output: write cycle OD = X; read cycle OD = L.

Common input/output: write cycle OD = H; read cycle OD = L.

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to 8,0 V
Input voltage range (any pin)	V_I	V_{SS} − 0,3 to V_{DD} +0,3 V
Operating temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

D.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 4,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 2,0 mA	V_{OH}	2,4	–	–	V

D.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 or 1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input voltage HIGH	V_{IH}	1,6	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,3	V
Output voltage HIGH at $-I_{OH}$ = 1,0 mA	V_{OH}	1,7	–	–	V

A.C. TEST CONDITIONS (V_{DD} = 5 V)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

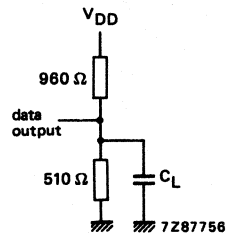


Fig. 4 Test load.

A.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 4 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	–	–	ns
Address access time	t_{AA}	–	–	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	150	ns
Chip enable CE2 to output	t_{CO2}	–	–	150	ns
Output disable OD to output	t_{OD}	–	–	70	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	150	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	–	–	ns
Chip enable CE2 to write	t_{CW2}	120	–	–	ns
Data set-up time	t_{DW}	70	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	70	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	70	–	–	ns

A.C. TEST CONDITIONS (V_{DD} = 3 V)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

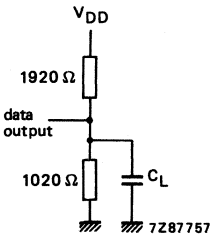


Fig. 5 Test load.

A.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; loads as per Fig. 5 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	–	–	ns
Address access time	t_{AA}	–	–	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	400	ns
Chip enable CE2 to output	t_{CO2}	–	–	400	ns
Output disable OD to output	t_{OD}	–	–	200	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	400	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	–	–	ns
Chip enable CE2 to write	t_{CW2}	300	–	–	ns
Data set-up time	t_{DW}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	200	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	200	–	–	ns

WAVEFORMS

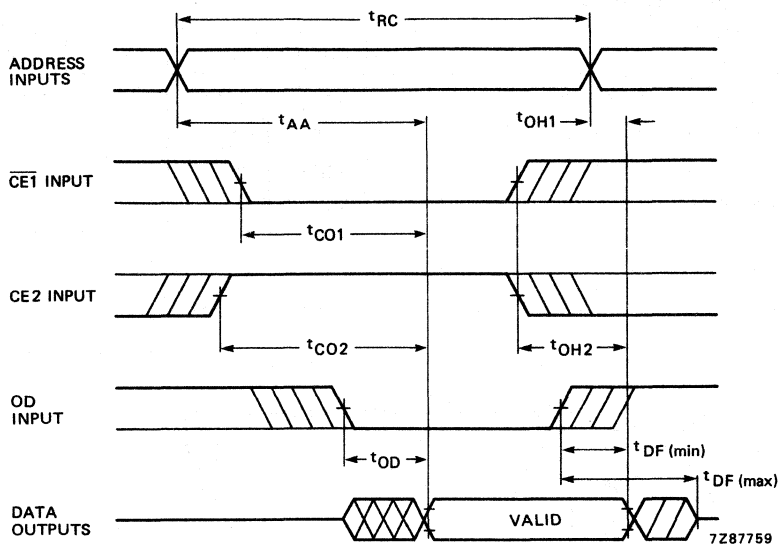


Fig. 6 Read cycle timing; R/$\overline{W}$ = HIGH.

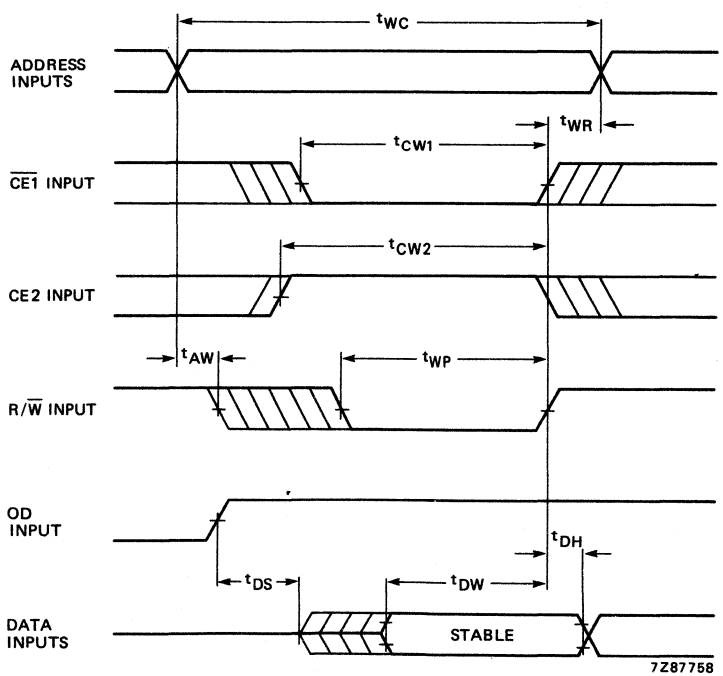


Fig. 7 Write cycle timing.

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

$CE2 \leqslant 0{,}2$ V; $T_{amb} = -25$ to $+70$ °C.

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	–	5,5	V
Data retention current at $V_{DD} = 1{,}5$ V	I_{DR}	–	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

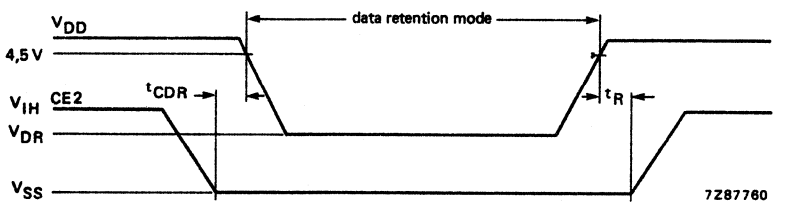


Fig. 8 Low supply voltage data retention characteristics.

1024 x 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5114 is a low-power, high-speed 4096-bit static CMOS RAM, organized as 1024 words of 4 bits each. The IC is suitable for low power and high speed applications, for battery operation and where battery backup is required. Inputs R/$\overline{W}$ and $\overline{CE}$ control the read/write operation and standby mode respectively. The PCD5114 is pin compatible with the SBB2114 types.

Features

- Operating supply voltage — 2,5 V to 5,5 V
- Low data retention voltage — min. 1,0 V
- Low standby current — max. 5 μA
- Cycle time = access time — max. 200 ns
- Static operation requiring no clock or timing strobe
- Low power consumption
- 3-state common data input/output interface
- All inputs and outputs directly TTL compatible
- Pin compatible with SBB2114 variants
- 18-lead DIL package
- 20-lead SO package

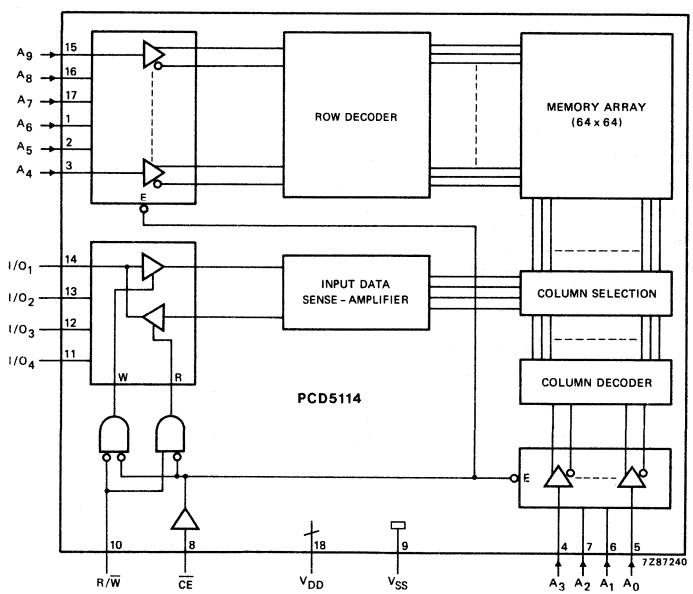


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD5114D: 18-lead DIL; ceramic (cerdip) (SOT-133B).
PCD5114P: 18-lead DIL; plastic (SOT-102G).
PCD5114T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

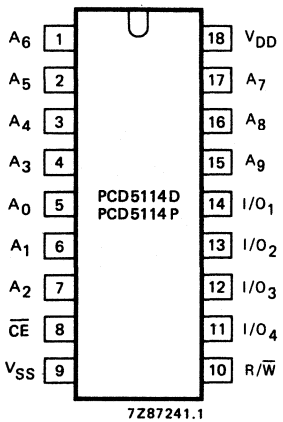


Fig. 2 Pinning diagram: PCD5114D; PCD5114P.

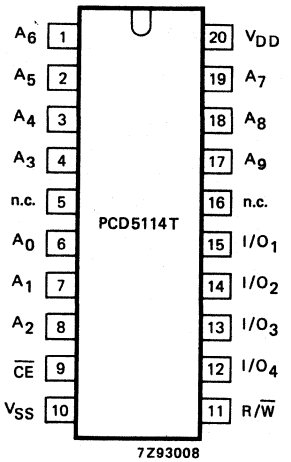


Fig. 3 Pinning diagram: PCD5114T.

A_0 to A_3	column address inputs
A_4 to A_9	row address inputs
$\overline{CE}$	chip enable input
$R/\overline{W}$	read/write input
I/O_1 to I/O_4	data input/output
V_{SS}	negative supply (ground)
V_{DD}	positive supply (+ 5 V)

Table 1 Mode selection

$\overline{CE}$	$R/\overline{W}$	mode	output	power
H	H	not selected	high impedance	standby
H	L	not selected	high impedance	standby
L	H	read	active	active
L	L	write	high impedance	active

H = HIGH logic level (the most positive voltage)
L = LOW logic level (the most negative voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 8 V
Input voltage range (any pin)	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−25 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 2 mA	V_{OH}	2,4	–	–	V
Output voltage LOW					
at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

D.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 V/1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	1,6	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 1 mA	V_{OH}	1,7	–	–	V
Output voltage LOW					
at I_{OL} = 1 mA	V_{OL}	–	–	0,3	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

A.C. CHARACTERISTICS

V_{DD} = 5 V ±0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; measured in Fig. 4, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	200	–	–	ns
Address access time	t_{AA}	–	–	200	ns
Chip select access time	t_{AC}	–	–	200	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	80	ns
Write cycle					
Write cycle time	t_{WC}	200	–	–	ns
Chip selection to end of write	t_{CW}	120	–	–	ns
Address set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	140	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	80	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	60	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 4)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load	2 TTL gates and C_L = 100 pF

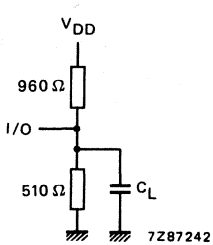


Fig. 4 Load for a.c. test conditions (V_{DD} = 5 V ± 0,5 V).

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70°C; measured in Fig. 5, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	500	–	–	ns
Address access time	t_{AA}	–	–	500	ns
Chip select access time	t_{AC}	–	–	500	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	200	ns
Write cycle					
Write cycle time	t_{WC}	500	–	–	ns
Chip selection to end of write	t_{CW}	300	–	–	ns
Adress set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	350	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	150	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 5)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	2 TTL gates and C_L = 100 pF

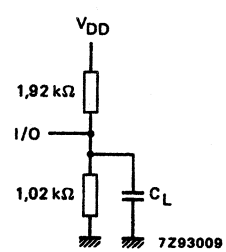


Fig. 5 Load for a.c. test conditions (V_{DD} = 3 V ± 0,5 V).

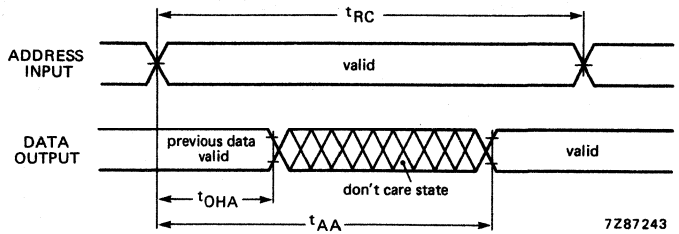


Fig. 6 Read cycle timing (1): R/$\overline{W}$ is HIGH; $\overline{CE}$ is LOW for a read cycle.

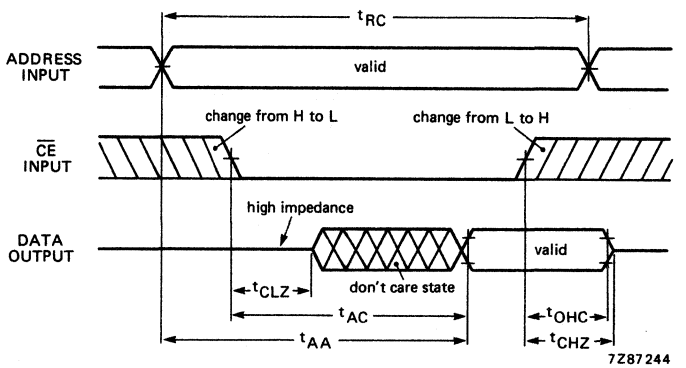


Fig. 7 Read cycle timing (2): R/$\overline{W}$ is HIGH for a read cycle.

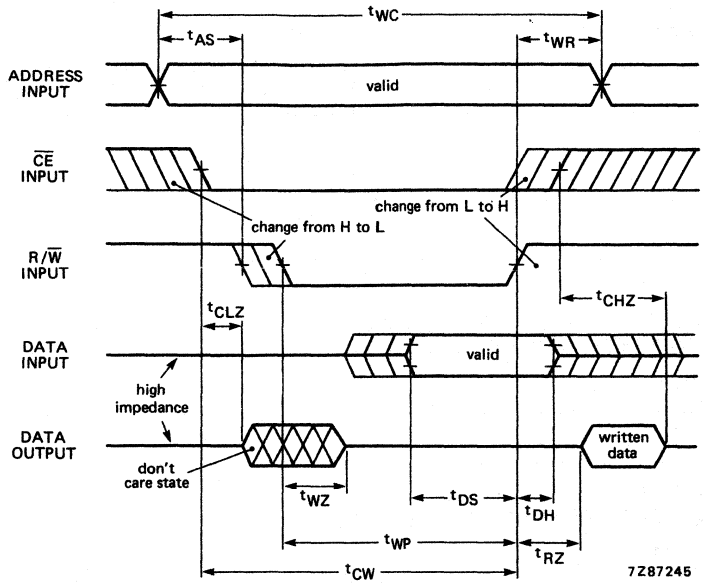


Fig. 8 Write cycle (1): R/$\overline{W}$ controlled.

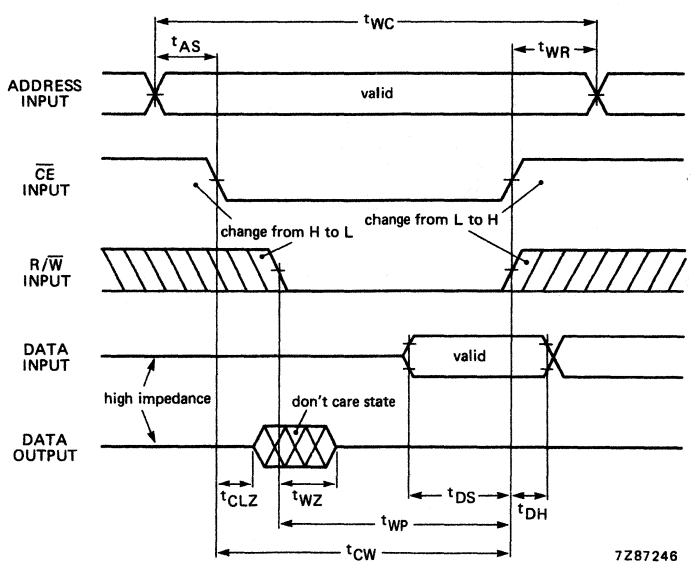


Fig. 9 Write cycle (2): $\overline{CE}$ controlled.

Note : If the $\overline{CE}$ low transition occurs after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.

DEVELOPMENT DATA

CAPACITANCE

$f = 1$ MHz; $T_{amb} = 25\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
Input capacitance at $V_I = V_{SS}$	C_I	–	–	5	pF
Output capacitance at $V_O = V_{SS}$	C_O	–	–	5	pF

LOW V_{DD} DATA RETENTION CHARACTERISTICS

$T_{amb} = -25$ to $+70\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
V_{DD} for data retention at $\overline{CE} = V_{DDR} \pm 0{,}2$ V; $V_I = V_{DDR}$ to V_{SS}	V_{DDR}	1	–	5,5	V
Data retention current at $V_{DDR} = 1{,}5$ V	I_{DDR}	–	0,02	2	μA
Chip deselect to data retention time	t_{CR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

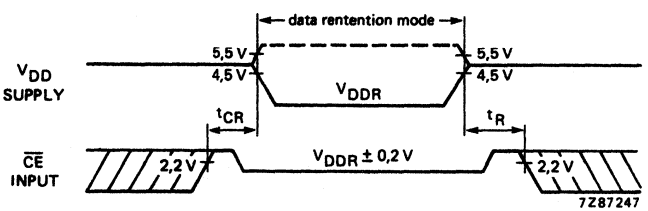


Fig. 10 LOW V_{DD} data retention.

256 x 8-BIT STATIC RAM WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcontroller families MAB8400 and PCF84C00

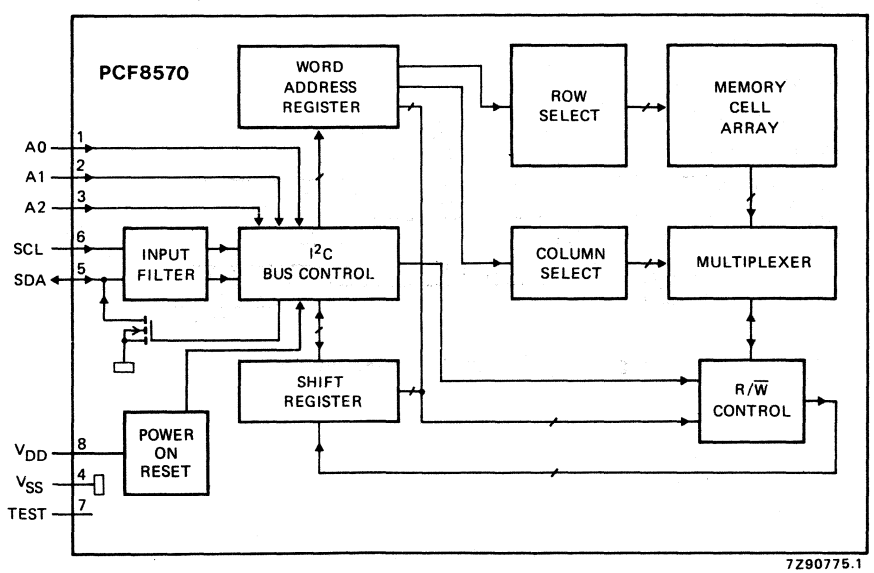


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570P: 8-lead DIL; plastic (SOT-97).
PCF8570T: 8-lead mini-pack plastic (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 14 and 15)
8	V_{DD}	positive supply

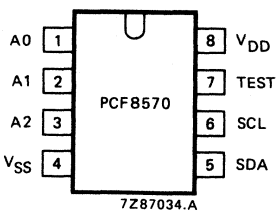


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}	−0,8 to + 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max. 10	mA
D.C. output current (any output)	$\pm I_O$	max. 10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}$; I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Figs 14 and 15)					
Supply current at T_{amb} = 25 °C; TEST = V_{DDR}	I_{DDR}	–	50	400	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

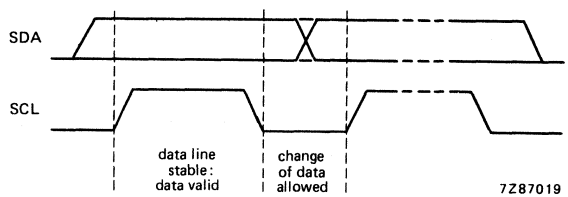


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

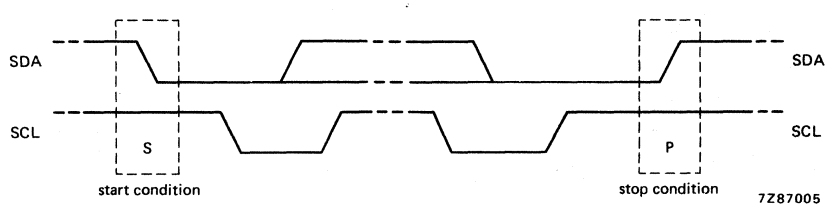


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

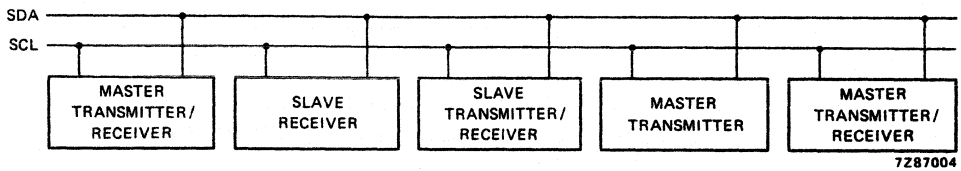


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

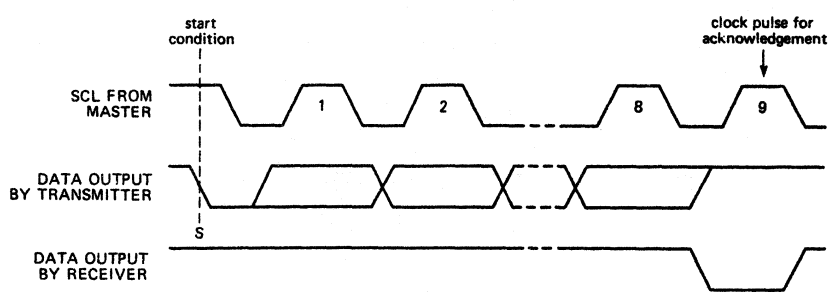


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

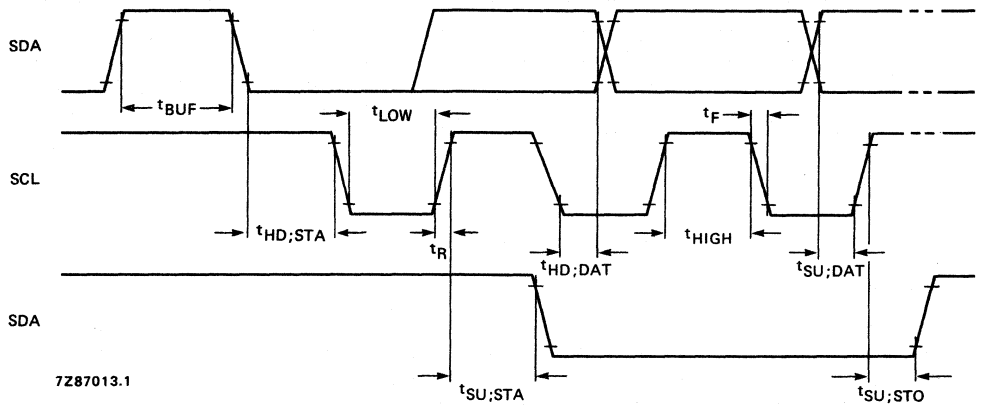


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

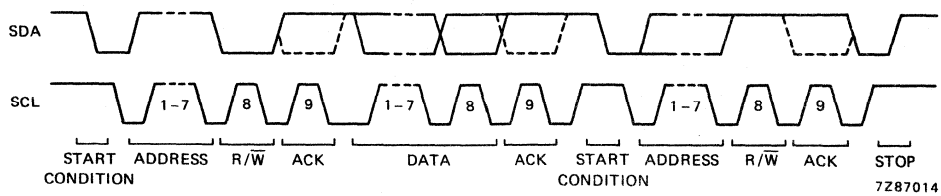


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

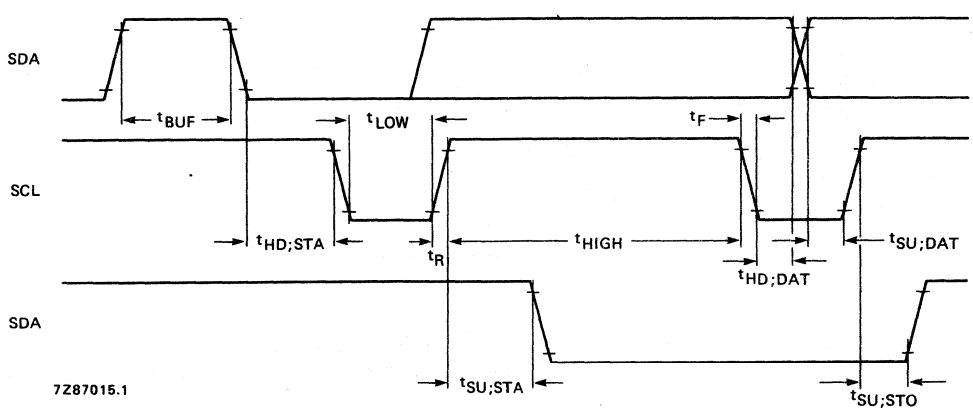


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

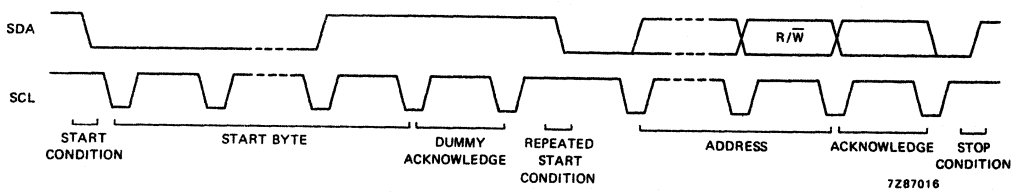


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Fig. 11.

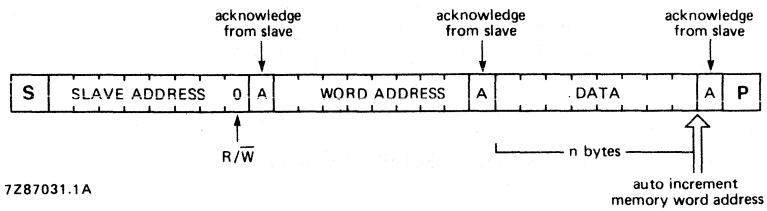


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

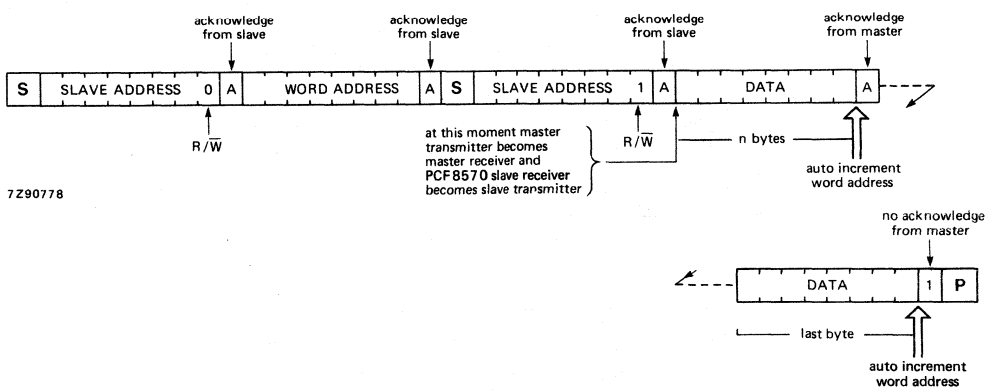


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

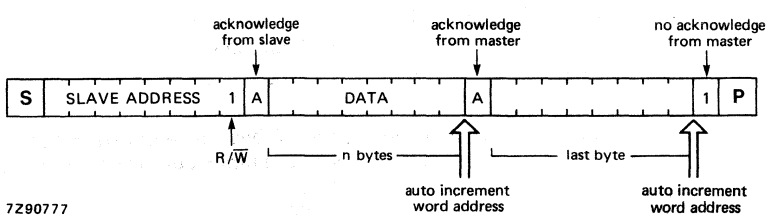


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

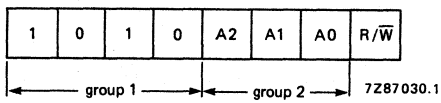


Fig. 12 PCF8570 address.

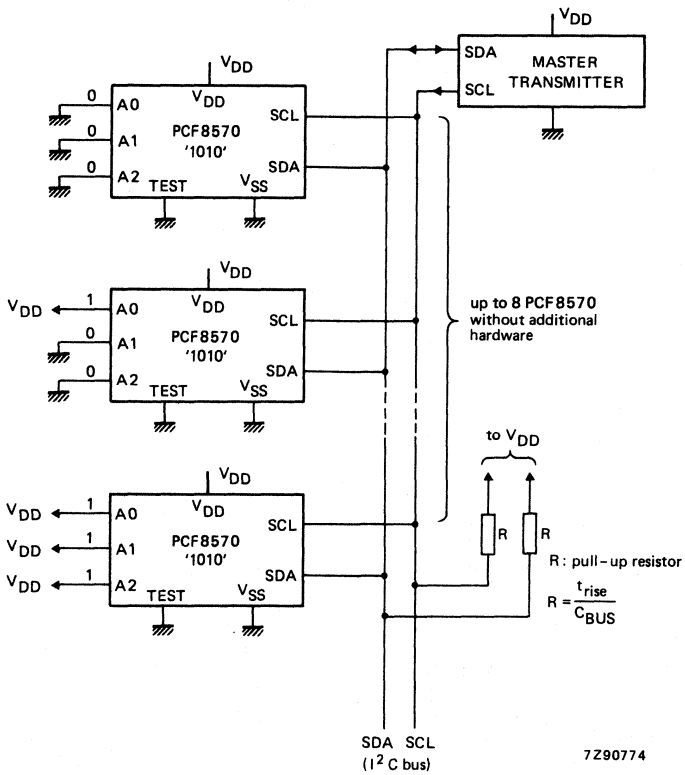


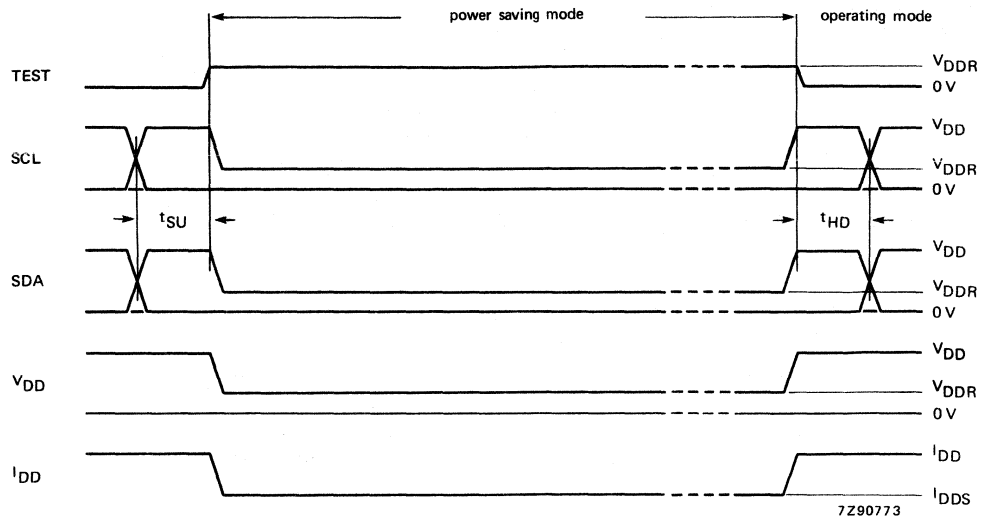
Fig. 13 PCF8570 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8570 goes into the power saving mode and the I²C bus logic is reset.



Where:

$t_{SU} \geqslant 4\ \mu s$

$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

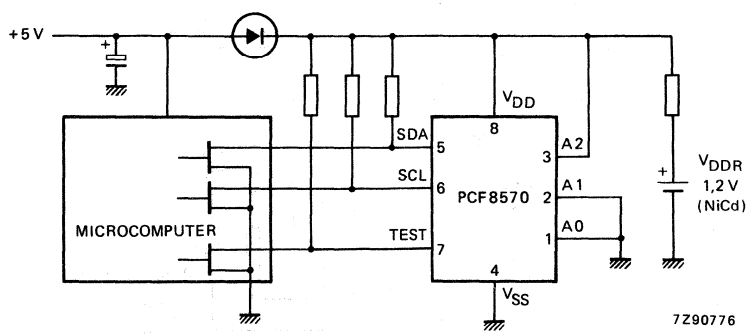
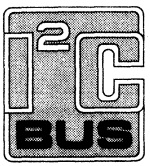


Fig. 15 Application example for power saving mode.

Note to Fig. 15

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

256 x 8-BIT STATIC RAM WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcomputer families MAB8400 and PCF84C00

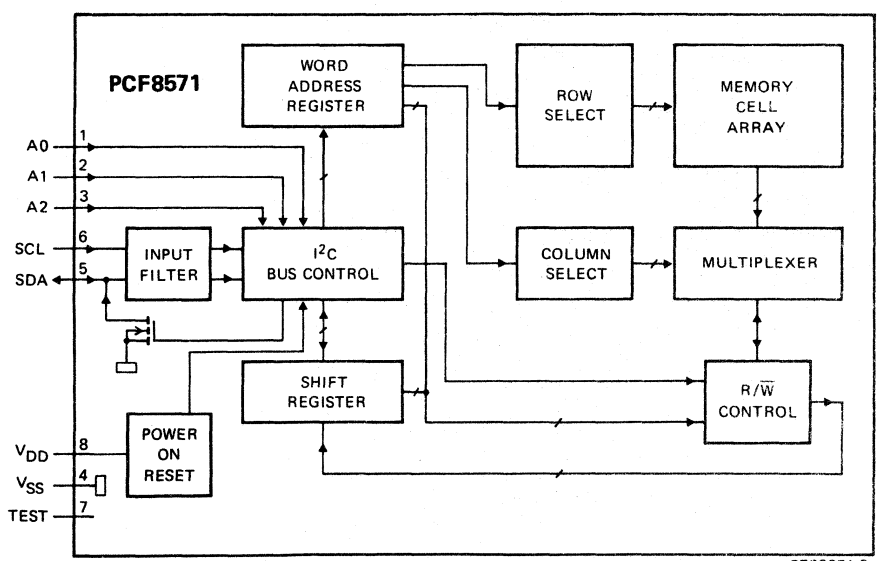


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8571P : 8-lead DIL; plastic (SOT-97).
PCF8571D : 8-lead DIL; ceramic (cerdip) (SOT-151A).
PCF8571T : 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Fig. 14 and 15)
8	V_{DD}	positive supply

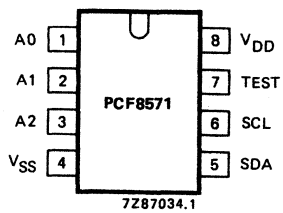


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max.	10	mA
D.C. output current (any output)	$\pm I_O$	max.	10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}; I_{SS}$	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating temperature range	T_{amb}		−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
$V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz;	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level					
at $V_{SCL} = V_{SDA} = V_{DD}$	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH					
at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current					
at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V;					
T_{amb} = −25 to 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 14)					
Supply current at T_{amb} = 25 °C;					
TEST = V_{DDR}	I_{DDS}	–	50	200	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

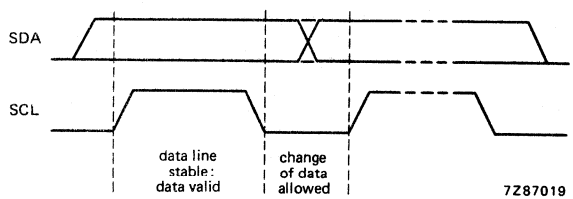


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

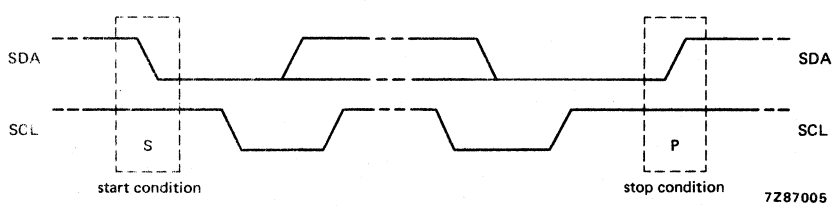


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

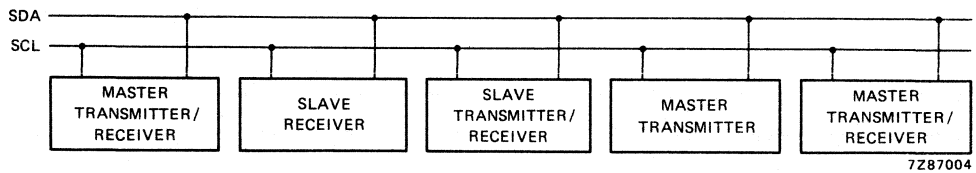


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

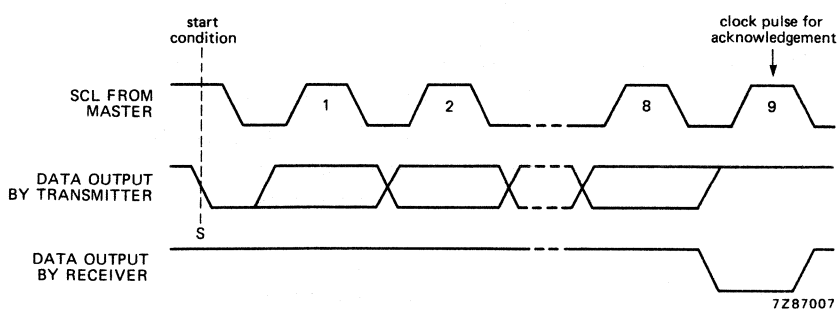


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8571 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

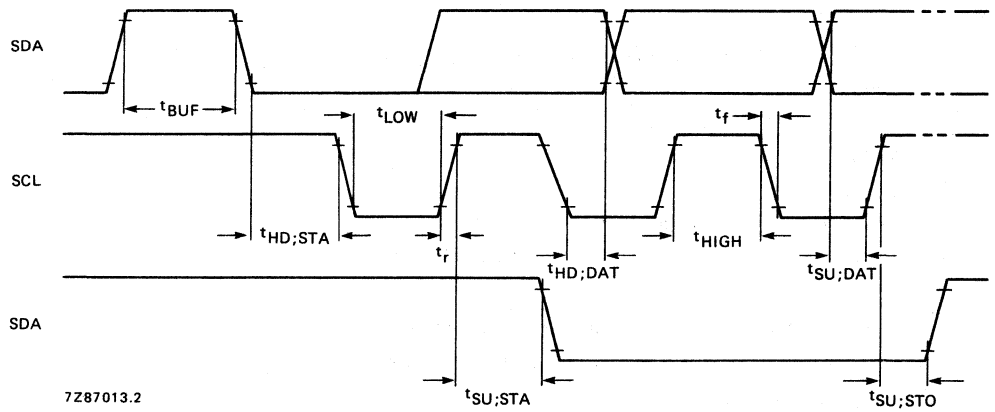


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

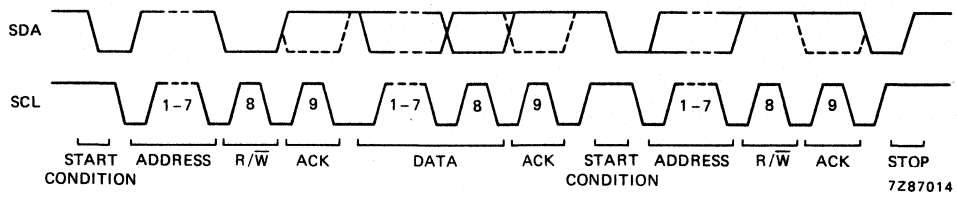


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

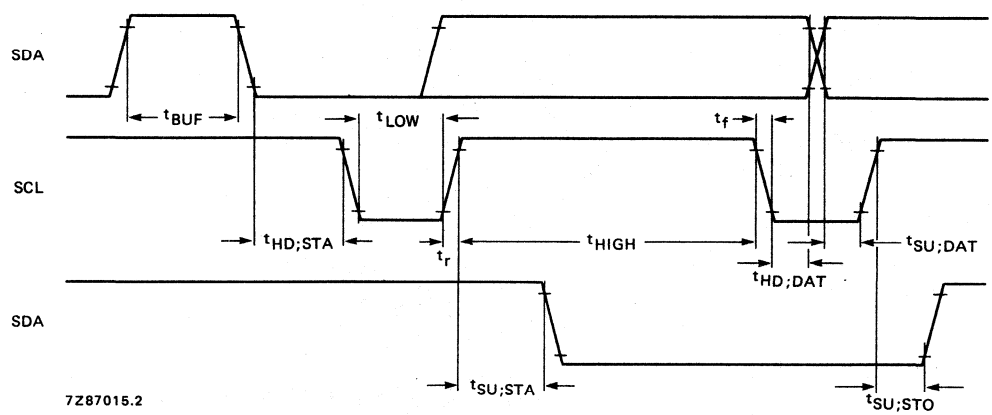


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250\ ns$
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300\ ns$
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

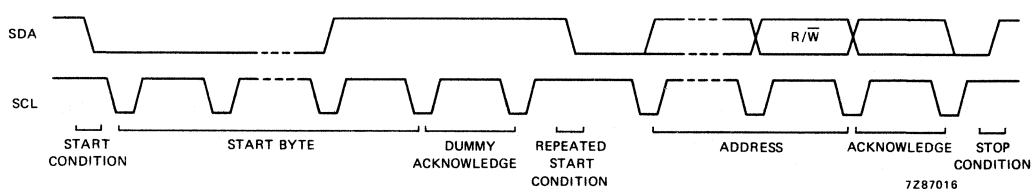


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8571 READ and WRITE cycles is shown in Fig. 11.

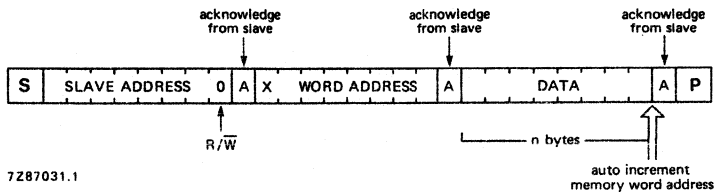


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

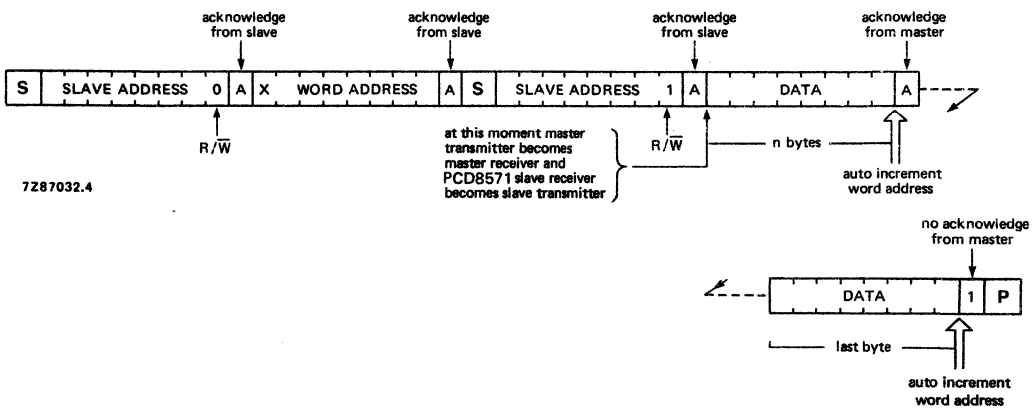


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

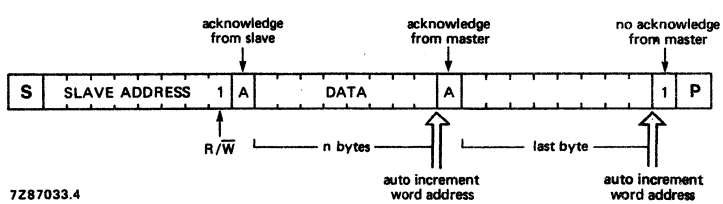


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

APPLICATION INFORMATION

The PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

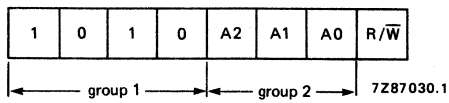


Fig. 12 PCF8571 address.

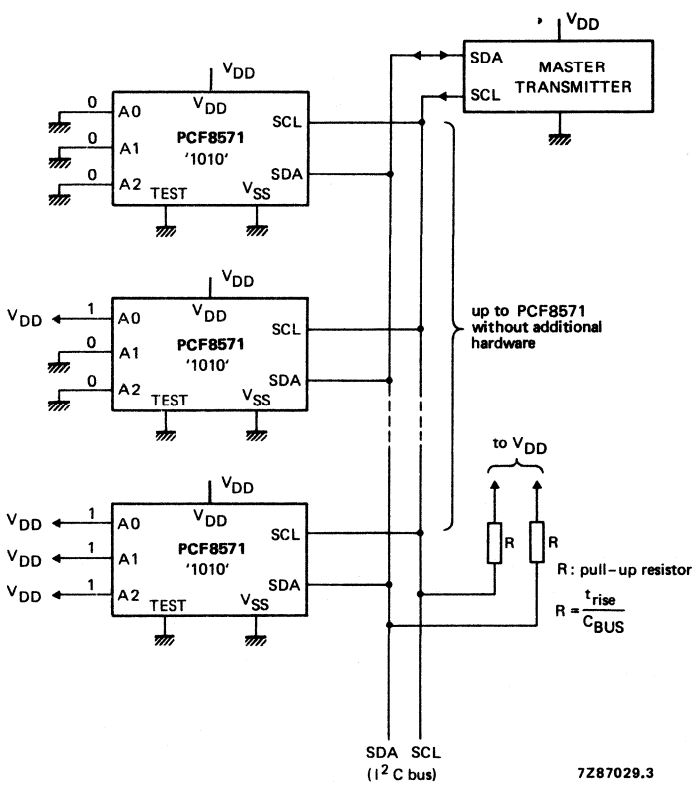


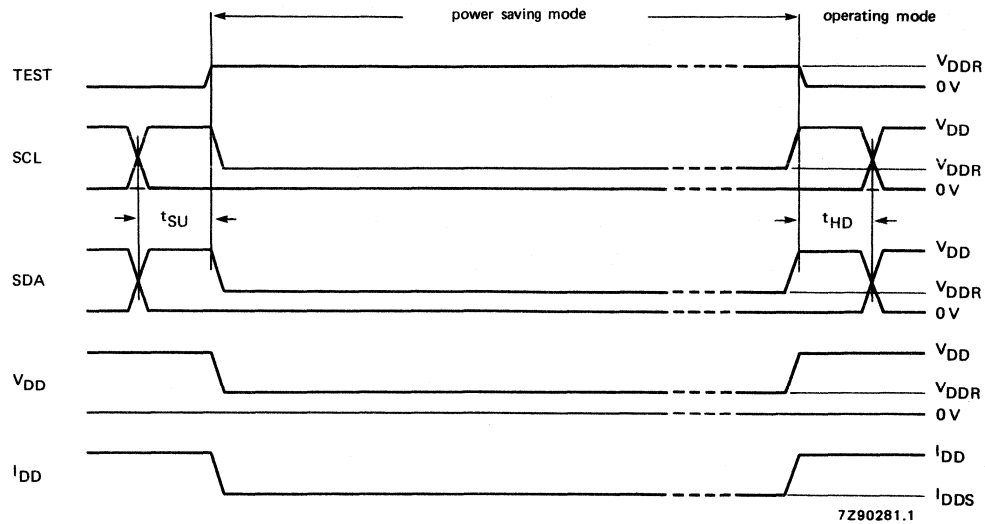
Fig. 13 PCF8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8571 goes into the power saving mode and I²C bus logic is reset.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

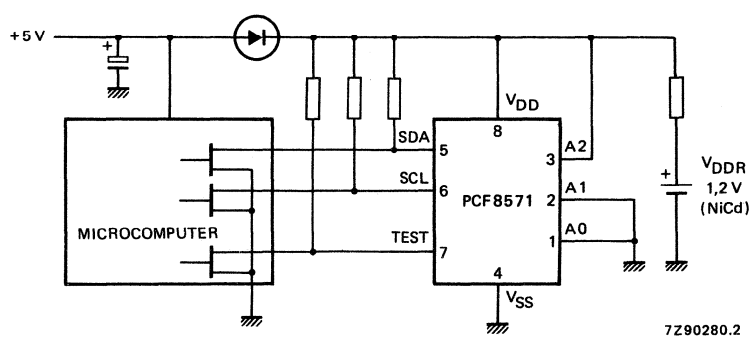
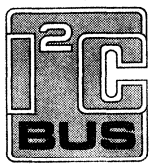


Fig. 15 Application example for power saving mode.

Note

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

256 x 8-BIT STATIC RAM WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I²C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

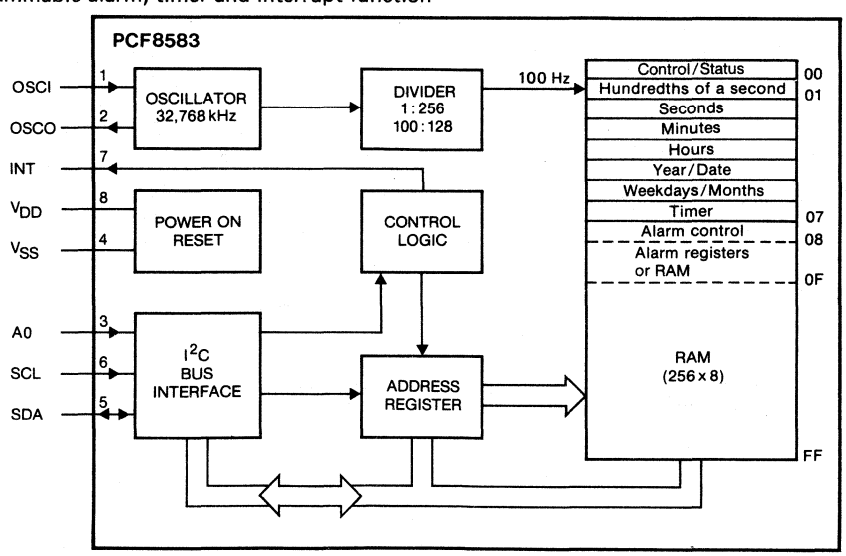


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT-97).
PCF8583T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C bus
6	SCL	serial clock line	I^2C bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

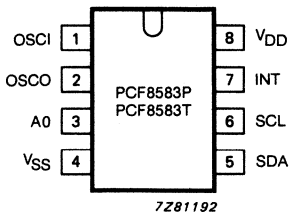


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V_{DD}		−0,8 to 8,0 V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8 V
D.C. input current (any input)	I_I	max.	10 mA
D.C. output current (any output)	I_O	max.	10 mA
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

Note

1. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I²C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

DEVELOPMENT DATA

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

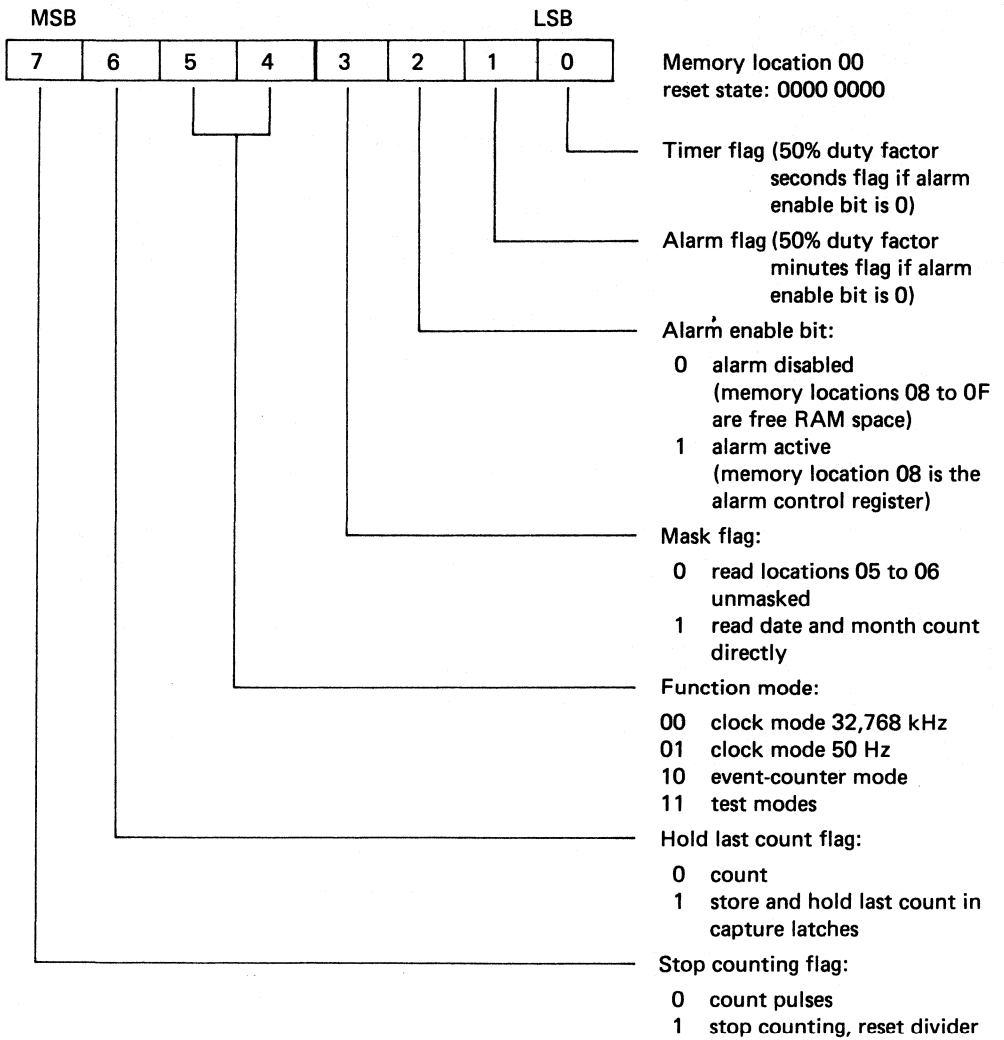


Fig. 3 Control/status register.

DEVELOPMENT DATA

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

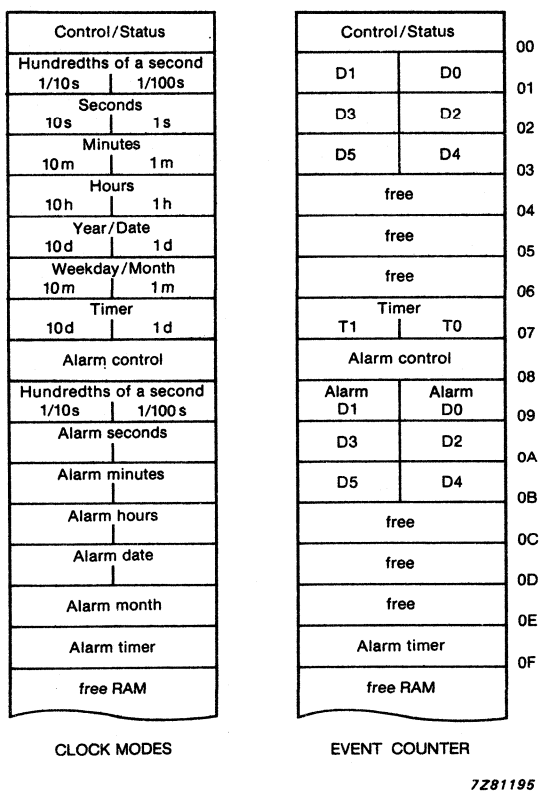
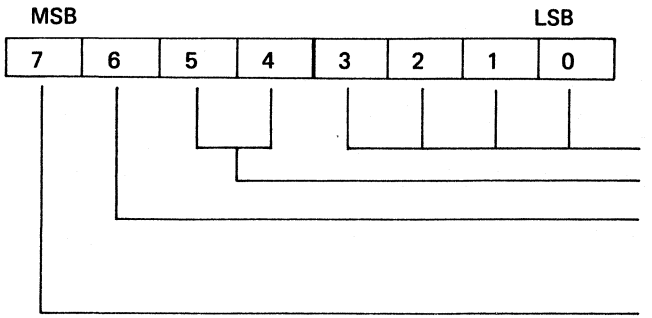


Fig. 4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

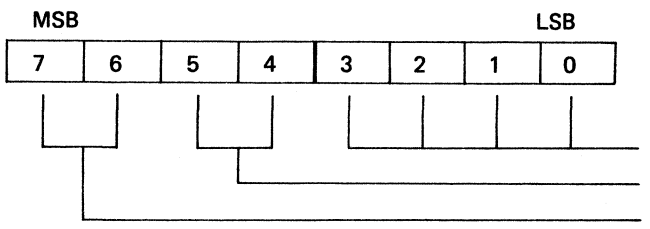
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig. 5 Format of the hours counter.



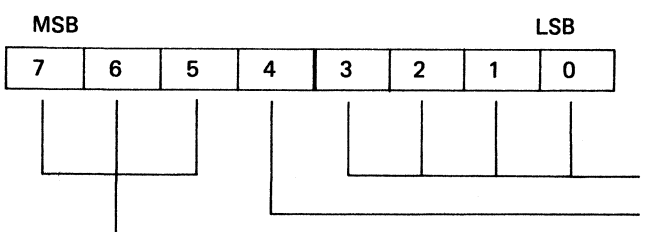
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig. 6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, 12
	01 to 30	30 to 01	4, 6, 9, 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

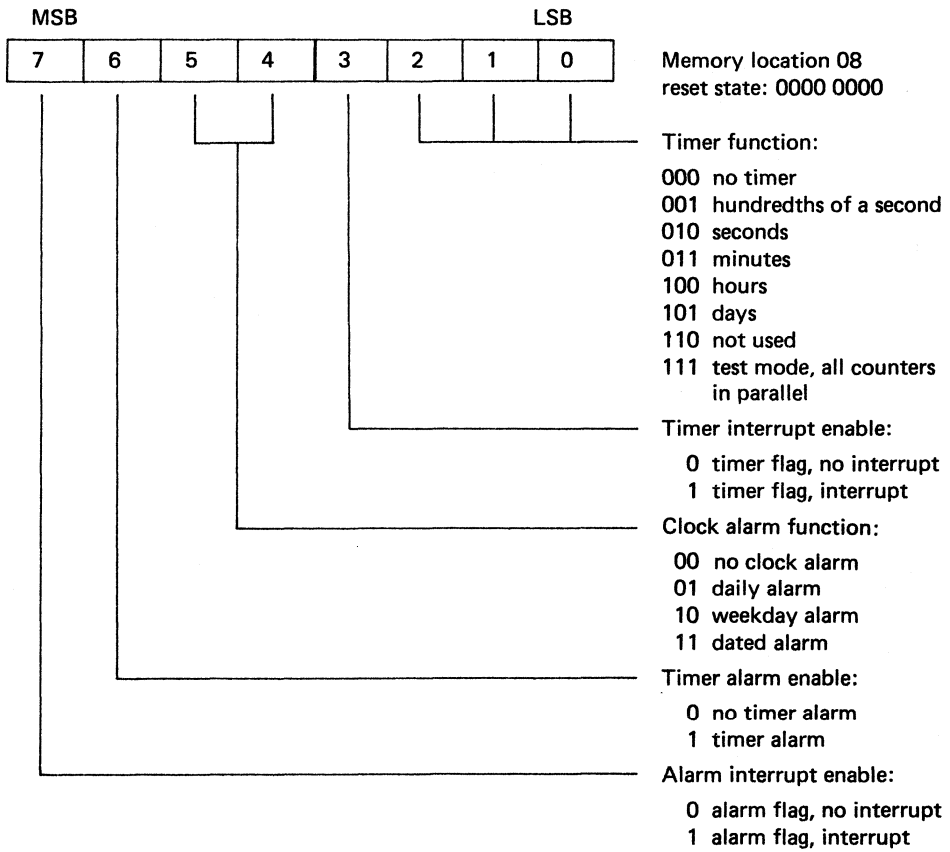
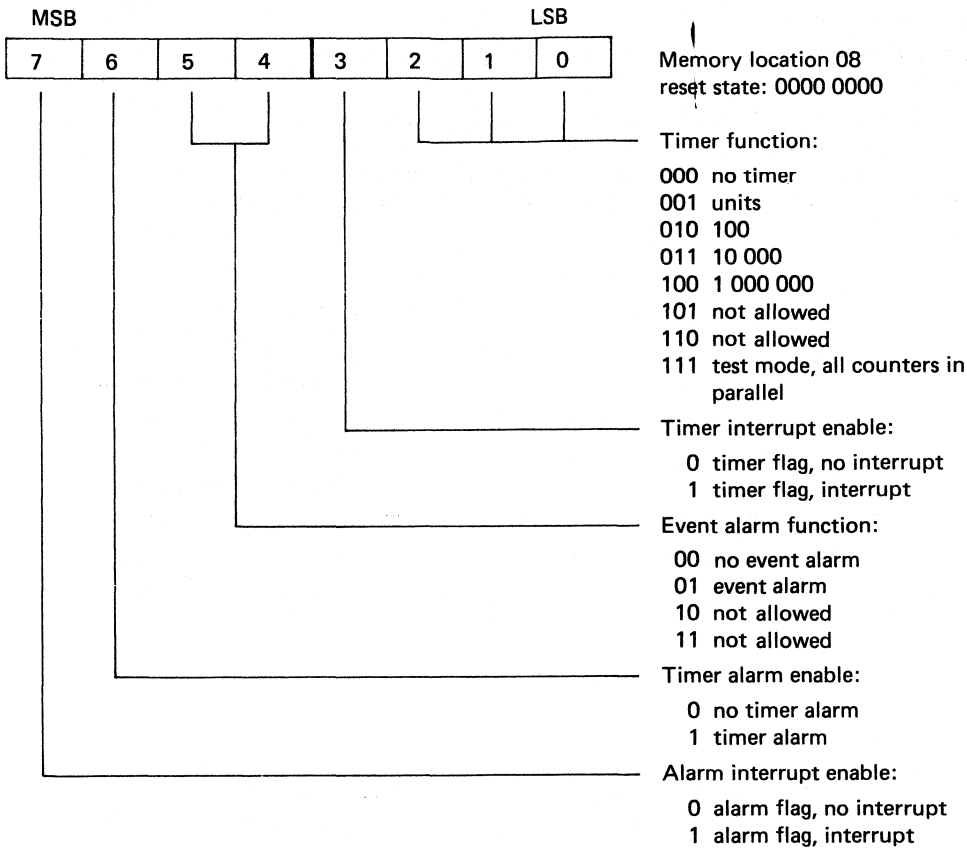


Fig. 8a Alarm control register, clock modes.



DEVELOPMENT DATA

Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

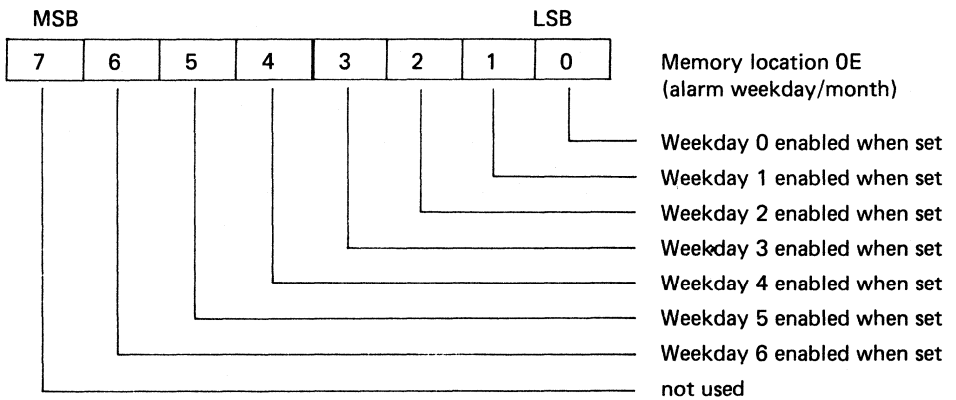


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I^2C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

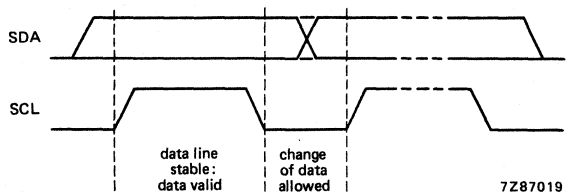


Fig. 10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

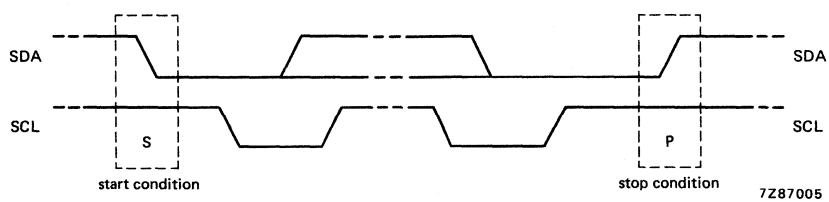


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

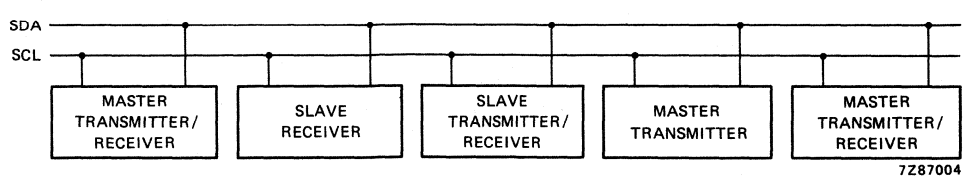


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

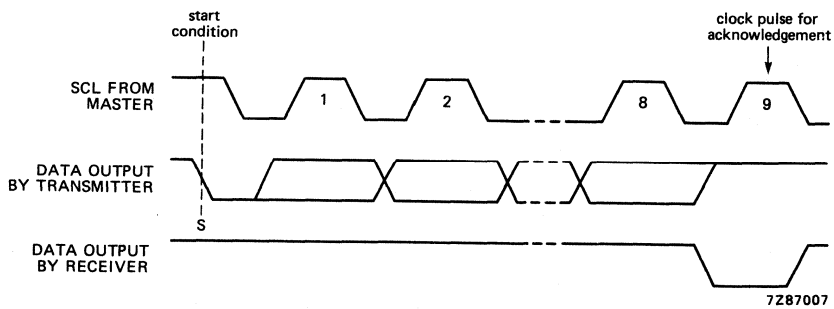


Fig. 13 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

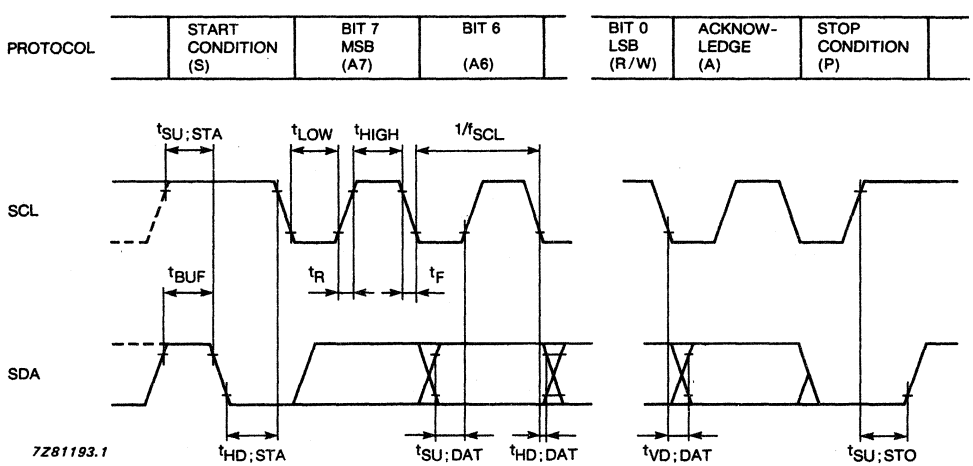


Fig. 14 I²C bus timing diagram.

I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

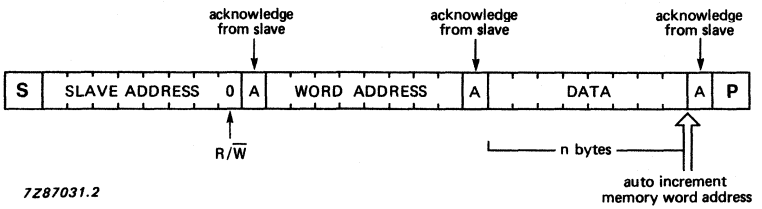


Fig. 15a Master transmits to slave receiver (WRITE mode).

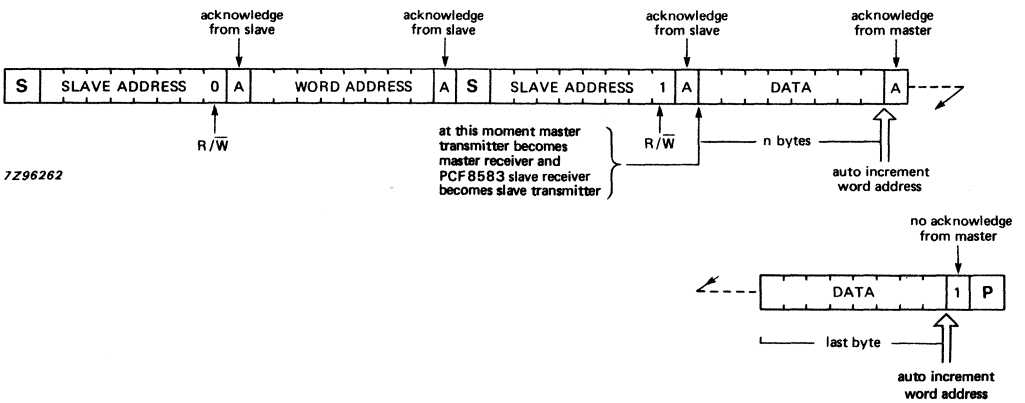


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

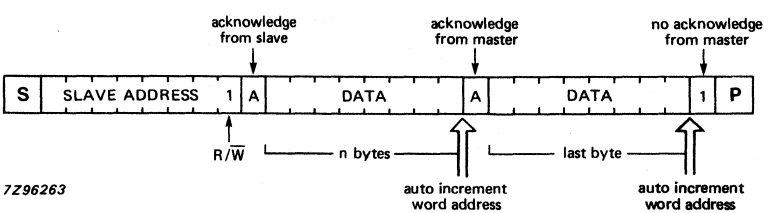


Fig. 15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2,0 to 6,0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit	
Supply						
Supply voltage (operating)	V_{DD}	2,5	–	6	V	←
Supply voltage (clock)	V_{DD}	1,0	–	6	V	←
Supply current						←
T_{amb} = 0 to 70 °C						←
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA	
Clock at V_{DD} = 5 V	I_{DDO}	–	10	50	μA	←
Clock at V_{DD} = 1 V	I_{DDO}	–	2	10	μA	
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V	
Inputs; input/output SDA						
Input voltage LOW (note 2)	V_{IL}	–0,8	–	0,3 x V_{DD}	V	
Input voltage HIGH (note 2)	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V	
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA	←
Output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA	
Input leakage current at V_I = V_{DD} or V_{SS}	± I_I	–	–	250	nA	
Input capacitance (SCL, SDA) at V_I = V_{SS}	C_I	–	–	7	pF	
LOW V_{DD} data retention						
Supply voltage for data retention	V_{DDR}	1	–	6	V	
Supply current at V_{DDR} = 1 V (note 3)	I_{DDR}	–	–	5	μA	←
Supply current at V_{DDR} = 1 V; T_{amb} = –25 to + 70 °C (note 3)	I_{DDR}	–	–	2	μA	←
Oscillator						
Integrated oscillator capacitance	C_{OSC}	–	40	–	pF	
Oscillator stability for: ΔV_{DD} = 100 mV at V_{DD} = 1,5 V; T_{amb} = 25 °C	f/f_{OSC}	–	2×10^{-6}	–	–	

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	KΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.
3. Event or 50 Hz mode only (no Quartz).

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

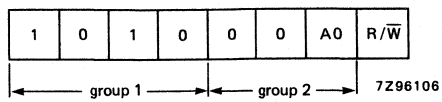


Fig. 16 PCF8583 address.

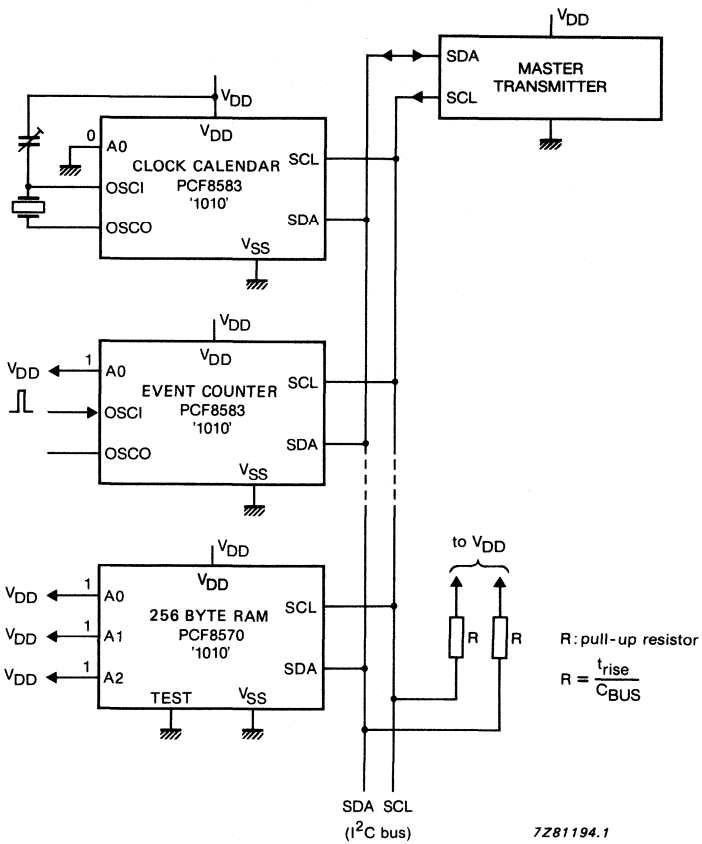
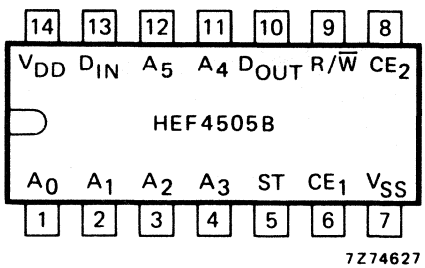


Fig. 17 PCF8583 application diagram.

64-BIT, 1-BIT PER WORD RANDOM ACCESS READ/WRITE MEMORY

The HEF4505B is a 64-bit, 1-bit per word, fully decoded and completely static, random access memory. The memory is strobed for reading or writing only when the strobe input (ST), chip enable inputs (CE_1 and CE_2) are HIGH simultaneously. The output data is available at the data output (D_{OUT}) only when the memory is strobed, the read/write input ($R/\overline{W}$) is HIGH and after the read access time has passed. Note that the three-state output is initially disabled and always goes to the LOW state before data is valid. The output is disabled in the high-impedance OFF-state, when the memory is not strobed or $R/\overline{W}$ is LOW. $R/\overline{W}$ may remain HIGH during a read cycle or LOW during a write cycle. The output data has the same polarity as the input data.



HEF4505BP : 14-lead DIL; plastic (SOT-27).
HEF4505BD: 14-lead DIL; ceramic (cerdip) (SOT-73).

Fig. 1 Pinning diagram.

PINNING

A_0 to A_5	address inputs
CE_1, CE_2	chip enable inputs
$R/\overline{W}$	read/write input
ST	strobe input
D_{IN}	data input
D_{OUT}	data output

FUNCTION TABLE

ST, CE_1, CE_2	$R/\overline{W}$	D_{OUT}	mode
L	L	Z	disabled
H	L	Z	write
L	H	Z	disabled
H	H	equal to memory data	read

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
Z = high-impedance OFF-state

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

Products approved to CECC 90 104-062.

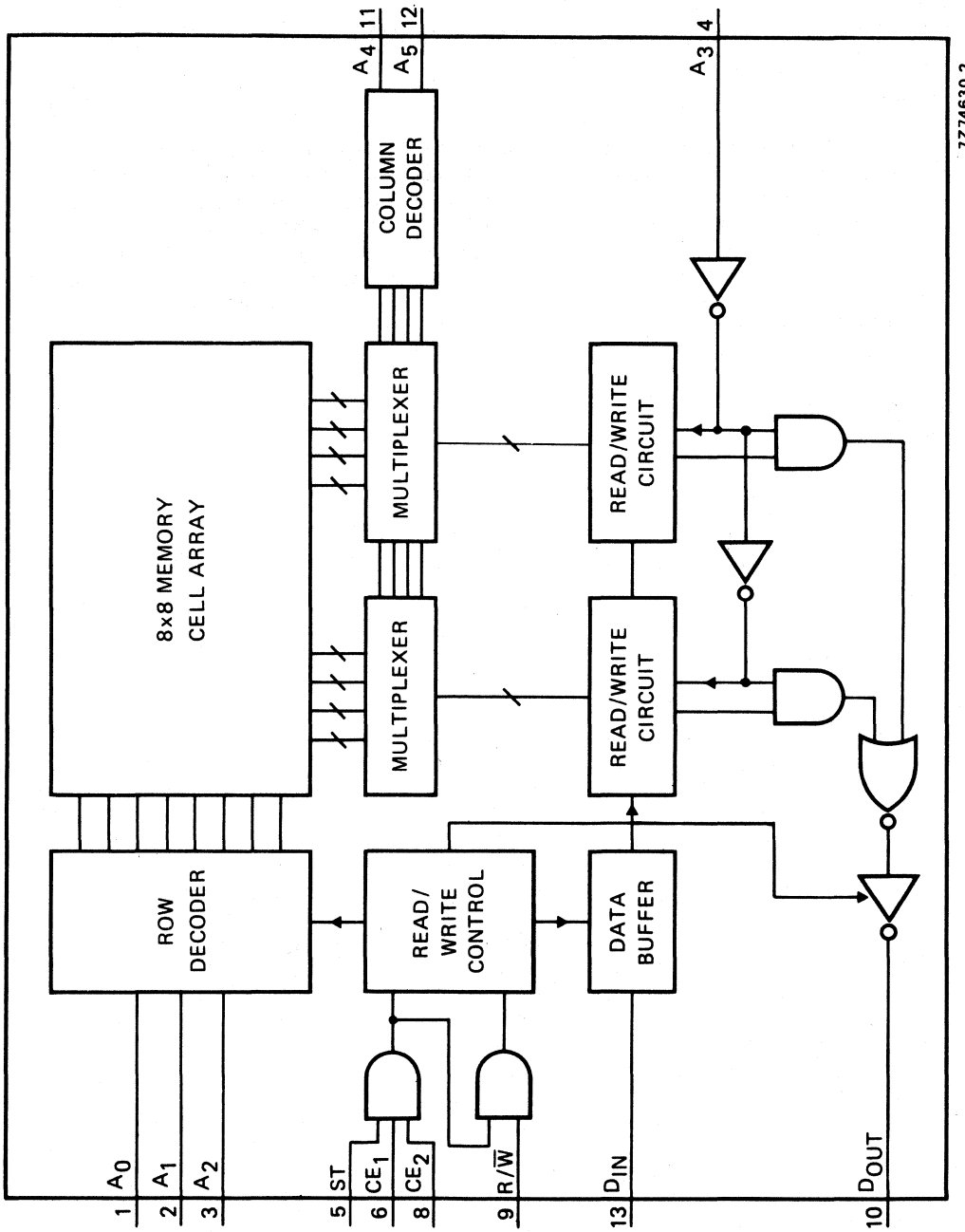
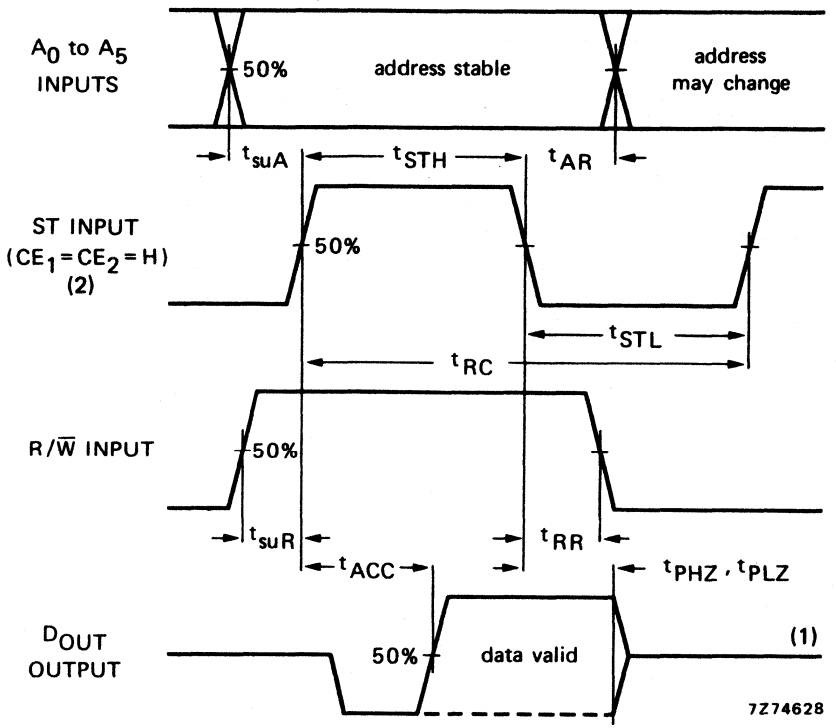


Fig. 2 Functional diagram.

A.C. CHARACTERISTICS

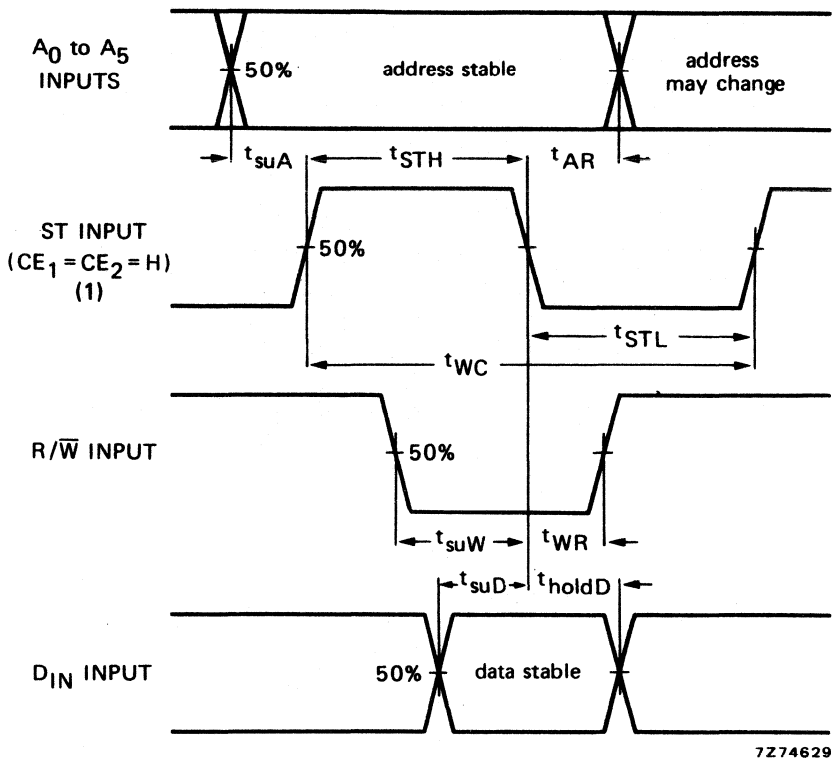
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Minimum strobe pulse width; LOW	5	t_{STL}	75	35		ns	
	10		45	22		ns	
	15		30	15		ns	
Read cycle time	5	t_{RC}		350	700	ns	
	10			250	500	ns	
	15			210	420	ns	
Write cycle time	5	t_{WC}		220	440	ns	
	10			125	250	ns	
	15			75	150	ns	
Read access time	5	t_{ACC}		330	660	ns	303 ns + (0,55 ns/pF) C_L
	10			135	270	ns	124 ns + (0,23 ns/pF) C_L
	15			100	200	ns	92 ns + (0,16 ns/pF) C_L
Address recovery time	5	t_{AR}	80	40		ns	
	10		40	20		ns	
	15		25	10		ns	
Read recovery time	5	t_{RR}	180	90		ns	
	10		120	60		ns	
	15		90	45		ns	
Write recovery time	5	t_{WR}	75	35		ns	
	10		45	25		ns	
	15		40	20		ns	
3-state propagation delays							
Output disable times	5	t_{PHZ}, t_{PLZ}		105	210	ns	
	10			60	125	ns	
	15			55	115	ns	
Set-up times							
$A_n \longrightarrow$ ST	5	t_{suA}	−20	−40		ns	
	10		−10	−20		ns	
	15		−5	−10		ns	
$R/\overline{W} \longrightarrow$ ST	5	t_{suR}	−30	−60		ns	
	10		−15	−30		ns	
	15		−5	−10		ns	
$D_{IN} \longrightarrow$ ST	5	t_{suD}	160	80		ns	
	10		75	35		ns	
	15		45	20		ns	
$R/\overline{W} \longrightarrow$ ST	5	t_{suW}	240	120		ns	
	10		100	50		ns	
	15		75	35		ns	
Hold time							
$D_{IN} \longrightarrow$ ST	5	t_{holdD}	−20	−40		ns	
	10		5	−10		ns	
	15		10	0		ns	



(1) Output in high impedance OFF-state.
(2) $t_{STHmin} = t_{RCmax} - t_{STLmin}$.

Fig. 3 Read cycle timing diagram.



(1) $t_{STHmin} = t_{WCmax} - t_{STLmin}$.

Fig. 4 Write cycle timing diagram.

APPLICATION INFORMATION

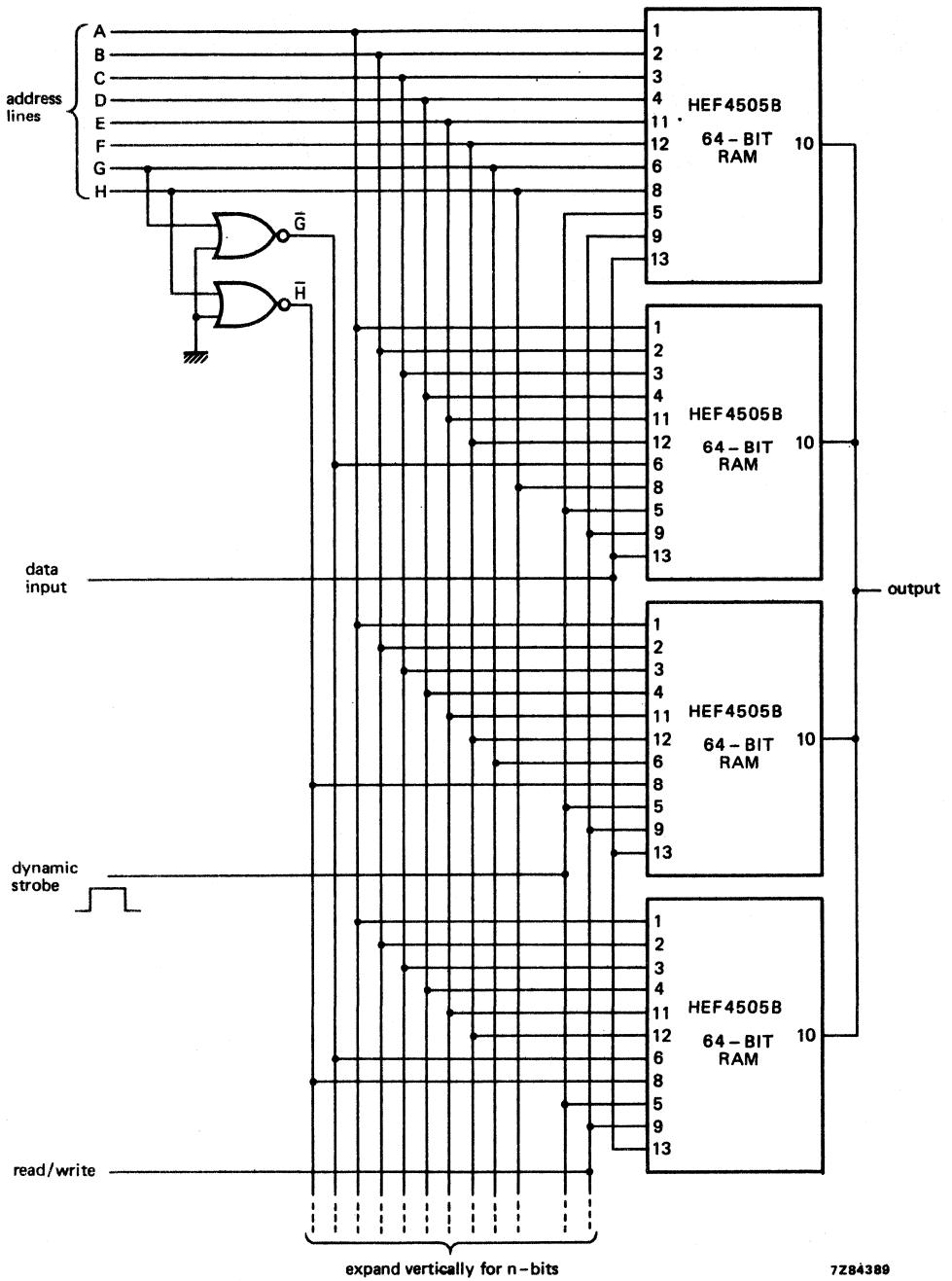


Fig. 5 256-word by n-bit static read/write memory using HEF4505B ICs.

Figure 5 shows a 256-word by n-bit static RAM system. The outputs of the four HEF4505B circuits are tied together to form 256 words by 1-bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and AND-ing them with the strobe input.

Fan-in and fan-out of the memory are limited only by speed requirements. The extremely low input and output leakage currents keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

The memory system shown in Fig. 5 can be interfaced directly with other ICs of the LOCMOS HE family. No external components are required.

Non-volatile information storage is allowed due to very low power dissipation when the memory is powered by a small standby battery. Figure 6 shows an optional standby power supply circuit for making a LOCMOS memory 'non-volatile'. When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor (R) which sets the charging rate. In Fig. 6 the sustaining voltage is V_B, and + V is the ordinary voltage from a power supply. V_{DD} is connected to the power supply pin of the memory. Low-leakage diodes are recommended to conserve battery power.

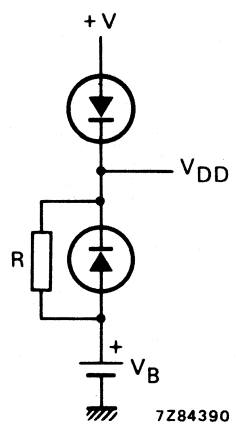


Fig. 6 Standby battery circuit.

256-BIT, 1-BIT PER WORD RANDOM ACCESS MEMORIES

The HEF4720B and HEF4720V are 256-bit, 1-bit per word random access memories with 3-state outputs. The memories are fully decoded and completely static.

Recommended supply voltage range for HEF4720B is 3 to 15 V and for HEF4720V is 4,5 to 12,5 V; minimum stand-by voltage for both types is 3 V.

The use of LOCMOS gives the added advantage of very low stand-by power. The circuits can be directly interfaced with standard bipolar devices (TTL) without using special interface circuits. The memory operates from a single power supply. The separate chip select input ($\overline{CS}$) allows simple memory expansion when the outputs are wire-ORed. If $\overline{CS}$ is HIGH, the outputs are floating and no new information can be written into the memory. The signal at O has the same polarity as the data input D, while the signal at $\overline{O}$ is the complement of the signal at O. The write control W must be HIGH for writing into the memory.

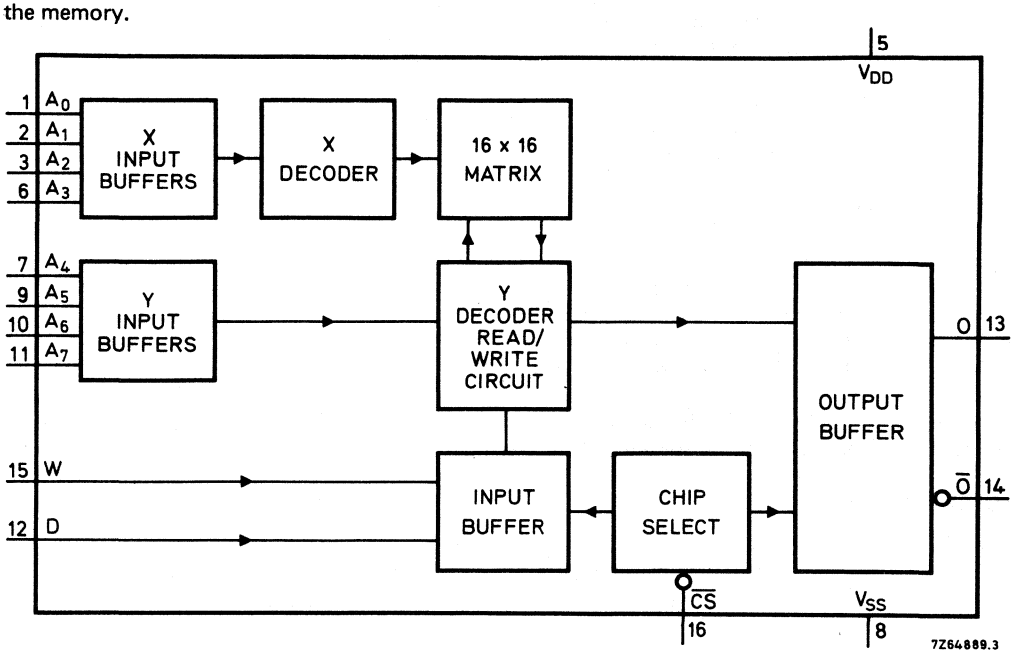


Fig. 1 Functional diagram.

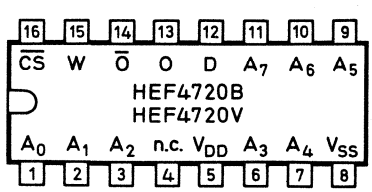


Fig. 2 Pinning diagram.

HEF4720BP; HEF4720VP: 16-lead DIL; plastic (SOT-38Z).
HEF4720BD; HEF4720VD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4720BT; HEF4720VT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

FAMILY DATA: see Family Specifications.

I_{DD} LIMITS: see next page.

FUNCTION TABLE

$\overline{CS}$	W	O	$\overline{O}$	mode
L	H	data written into memory	complement of data written into memory	write
L	L	data written into memory	complement of data written into memory	read
H	X	Z	Z	inhibit

H = HIGH state (the more positive voltage) X = state is immaterial
L = LOW state (the less positive voltage) Z = high impedance OFF-state

PINNING

$\overline{CS}$	chip select input (active LOW)
W	write enable input
D	data input
A_0 to A_7	address inputs
O	3-state output (active HIGH)
$\overline{O}$	3-state output (active LOW)

SUPPLY VOLTAGE

	rating	recommended operating	stand-by min.	
HEF4720B	−0,5 to 18	3,0 to 15,0	3	V
HEF4720V	−0,5 to 18	4,5 to 12,5	3	V

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4720V, because of its lower supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output current LOW	4,75	0,4		2,4		2		1,6		mA
	10	0,5	I_{OL}	4,8		4		3,2		mA
	15	1,5		10,0		10		7,5		mA
Quiescent device current	5				25		25		200	μA
	10		I_{DD}		50		50		400	μA
	15				100		100		800	μA
Input leakage current										
HEF4720V	10				0,3		0,3		1	μA
HEF4720B	15		$\pm I_{IN}$		0,3		0,3		1	μA

A.C. CHARACTERISTICS

	V_{DD} V	symbol	min.	typ.	max.		
Output capacitance	5	C_O		5		pF	
	10			5		pF	
	15			5		pF	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Read cycle							
Read access time	5	t_{ACC}		320	580	ns	292 ns + (0,55 ns/pF) C_L
	10			130	220	ns	118 ns + (0,23 ns/pF) C_L
	15			100	160	ns	92 ns + (0,16 ns/pF) C_L
Chip select to output time	5	t_{CO}			180	ns	
	10				70	ns	
	15				50	ns	
Address hold time	5	t_{OA}	0			ns	
	10		0			ns	
	15		0			ns	
Output hold time with respect to address input	5	t_{VAL1}	60	170		ns	142 ns + (0,55 ns/pF) C_L
	10		20	50		ns	38 ns + (0,23 ns/pF) C_L
	15		15	40		ns	32 ns + (0,16 ns/pF) C_L
Output hold time with respect to chip select input	5	t_{COH}			130	ns	
	10				70	ns	
	15				60	ns	
Output floating time with respect to chip select input	5	t_{COF}	0			ns	
	10		0			ns	
	15		0			ns	
Read cycle time	5	t_{RC}	580			ns	
	10		220			ns	
	15		160			ns	
Output transition times LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
HIGH to LOW	5	t_{THL}		40	80	ns	14 ns + (0,52 ns/pF) C_L
	10			22	40	ns	11 ns + (0,22 ns/pF) C_L
	15			15	30	ns	7 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	
Write cycle						
Write cycle time	5	t_{WC}	580			ns
	10		220			ns
	15		160			ns
Address to write set-up time	5	t_{AW}	110			ns
	10		50			ns
	15		50			ns
Write pulse width	5	t_{WP}	370		10 000	ns
	10		130		10 000	ns
	15		80		10 000	ns
Write recovery time	5	t_{WR}	100			ns
	10		40			ns
	15		30			ns
Data set-up time	5	t_{DW}	250			ns
	10		100			ns
	15		80			ns
Data hold time	5	t_{DH}	100			ns
	10		30			ns
	15		20			ns
Chip select set-up time with respect to write pulse	5	t_{CSW}	370			ns
	10		130			ns
	15		80			ns
Chip select hold time with respect to write pulse	5	t_{CSH}	0			ns
	10		0			ns
	15		0			ns
Chip select lead time over write pulse to prevent writing	5	t_{CSL}	0			ns
	10		0			ns
	15		0			ns
Read-modify-write cycle						
Read enable hold time	5	t_{RH}	0			ns
	10		0			ns
	15		0			ns
Output hold time with respect to write pulse	5	t_{VAL2}	60			ns
	10		20			ns
	15		15			ns
Read-modify-write cycle time	5	t_{RWC}	1050			ns
	10		390			ns
	15		270			ns

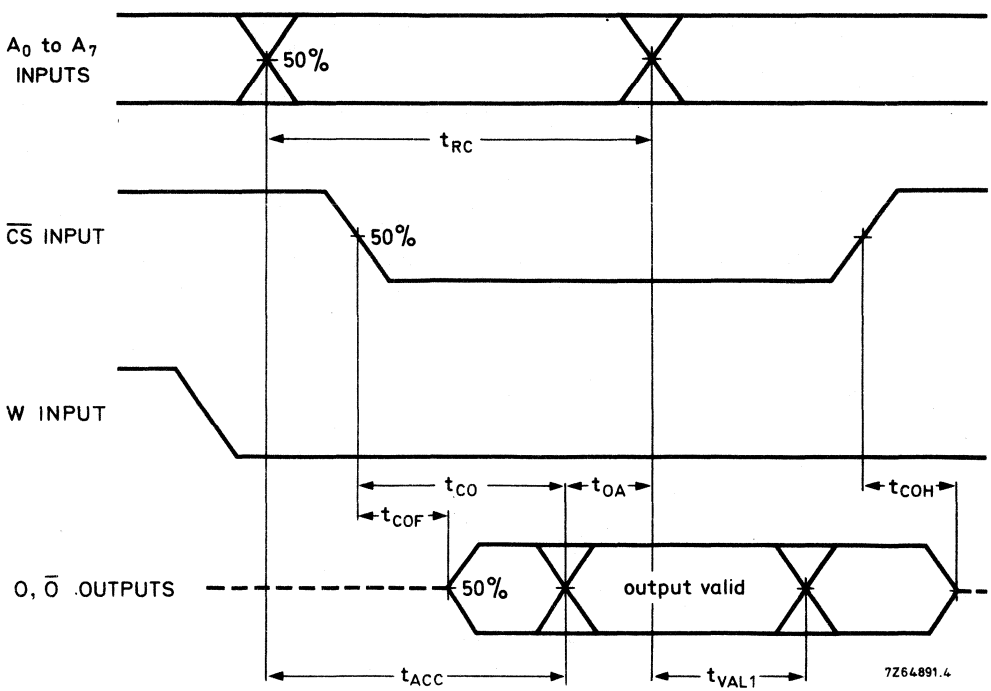


Fig. 3 Read cycle timing diagram.

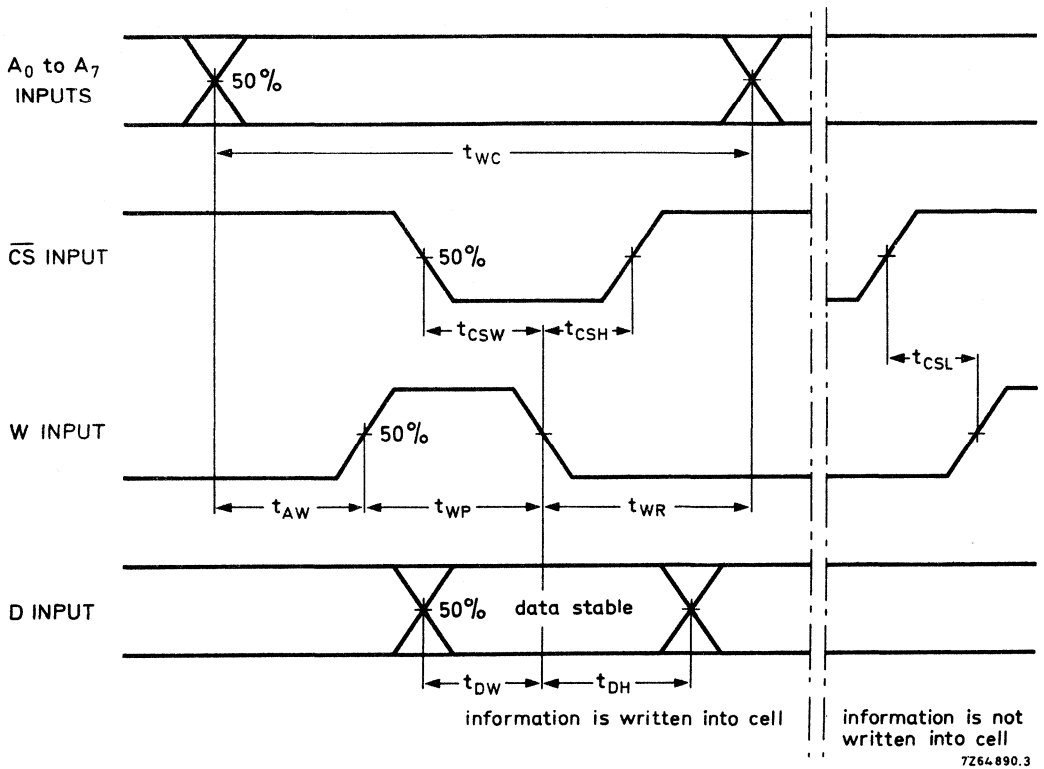


Fig. 4 Write cycle timing diagram.

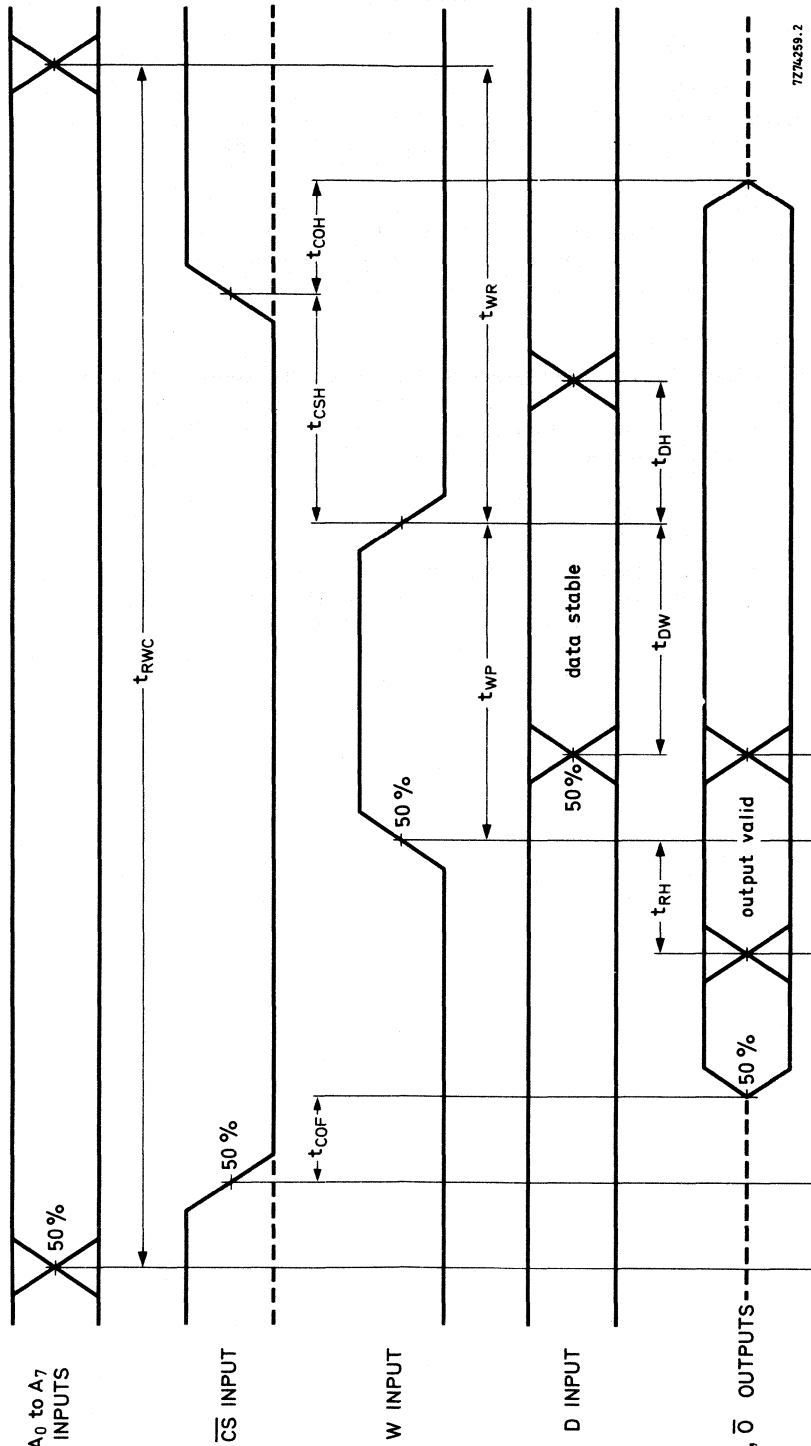


Fig. 5 Read-modify-write cycle timing diagram.

APPLICATION INFORMATION

Extension of memory capacity

The memory capacity of the HEF4720B; V is 256 bits (or 256 words of 1 bit). The capacity of a system can be extended in various ways by the connection of further HEF4720B; V ICs.

Extending the word length

By connecting a number of HEF4720B; V ICs as shown in Fig. 6, the word length (i.e. bits per word) is multiplied by that number. That is, each device stores 1 bit per word but the total number of words remains 256. For example, if four devices are used in this way, 256 four-binary-bit words can be stored.

Extending the number of words

If a number of HEF4720B; V ICs are connected as shown in Fig. 7, the words available are multiplied by that number, but the word length remains 1 bit. Notice that in this case additional addresses are used in conjunction with the $\overline{CS}$ input. In the case shown in Fig. 7 (4 x HEF4720B; V in parallel), the addresses and data inputs are loaded with four inputs (= 20 pF), the $\overline{CS}$ inputs are loaded with one input each.

Extending both the word length and number of words

Figure 8 shows how a combination of the extensions described above can be used to obtain both greater word length and additional words. It is clear that the capacitive load of the driving circuits puts a limit to the free choice of the interface. In Fig. 8, each address is loaded with 16 inputs, i.e. 16 x 5 = 80 pF: each CS inverter is loaded with 8 inputs, i.e. 8 x 5 = 40 pF. The data inverters in this case are loaded with only two inputs each.

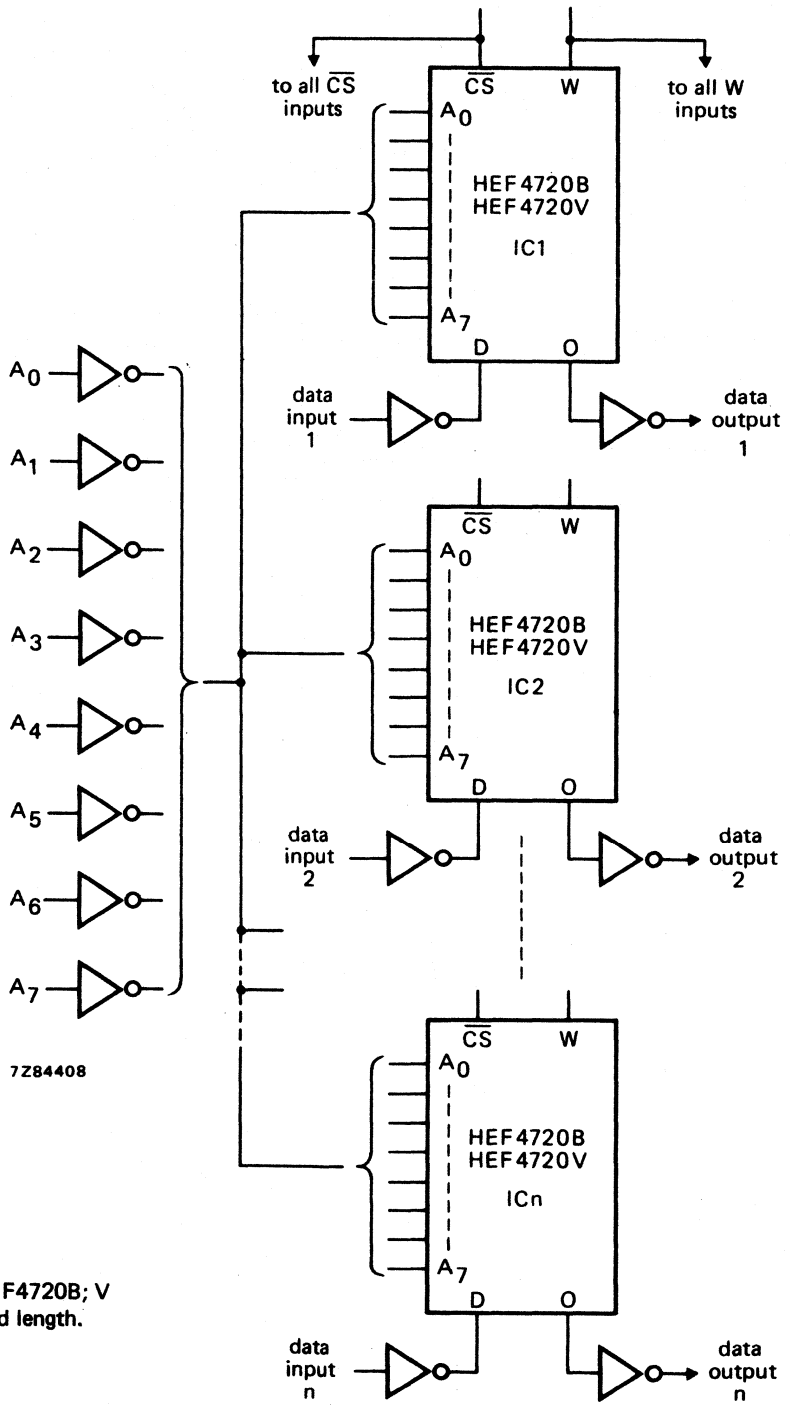


Fig. 6 Using extra HEF4720B; V ICs to extend the word length.

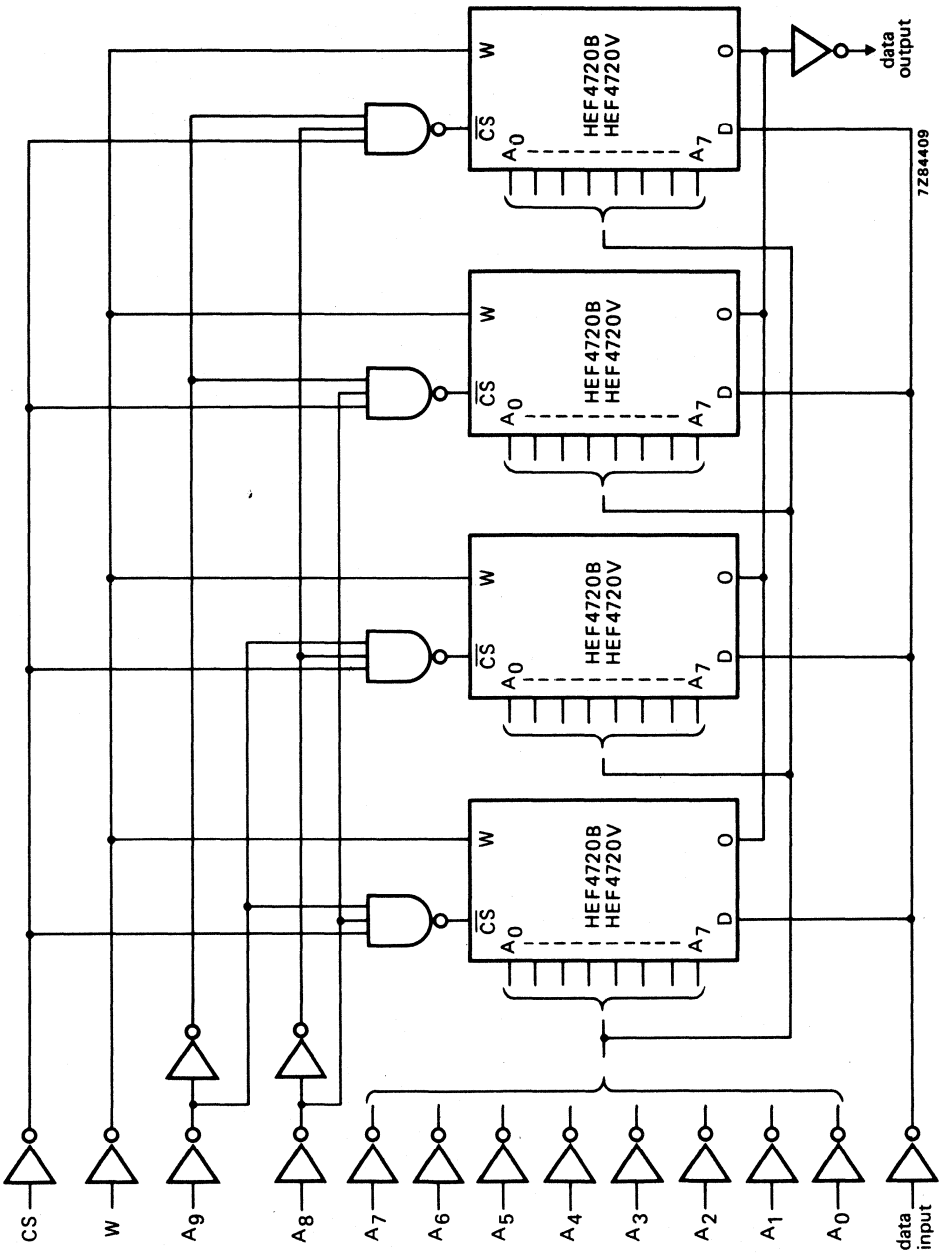


Fig. 7 Using extra HEF4720B; V ICs to obtain more words.

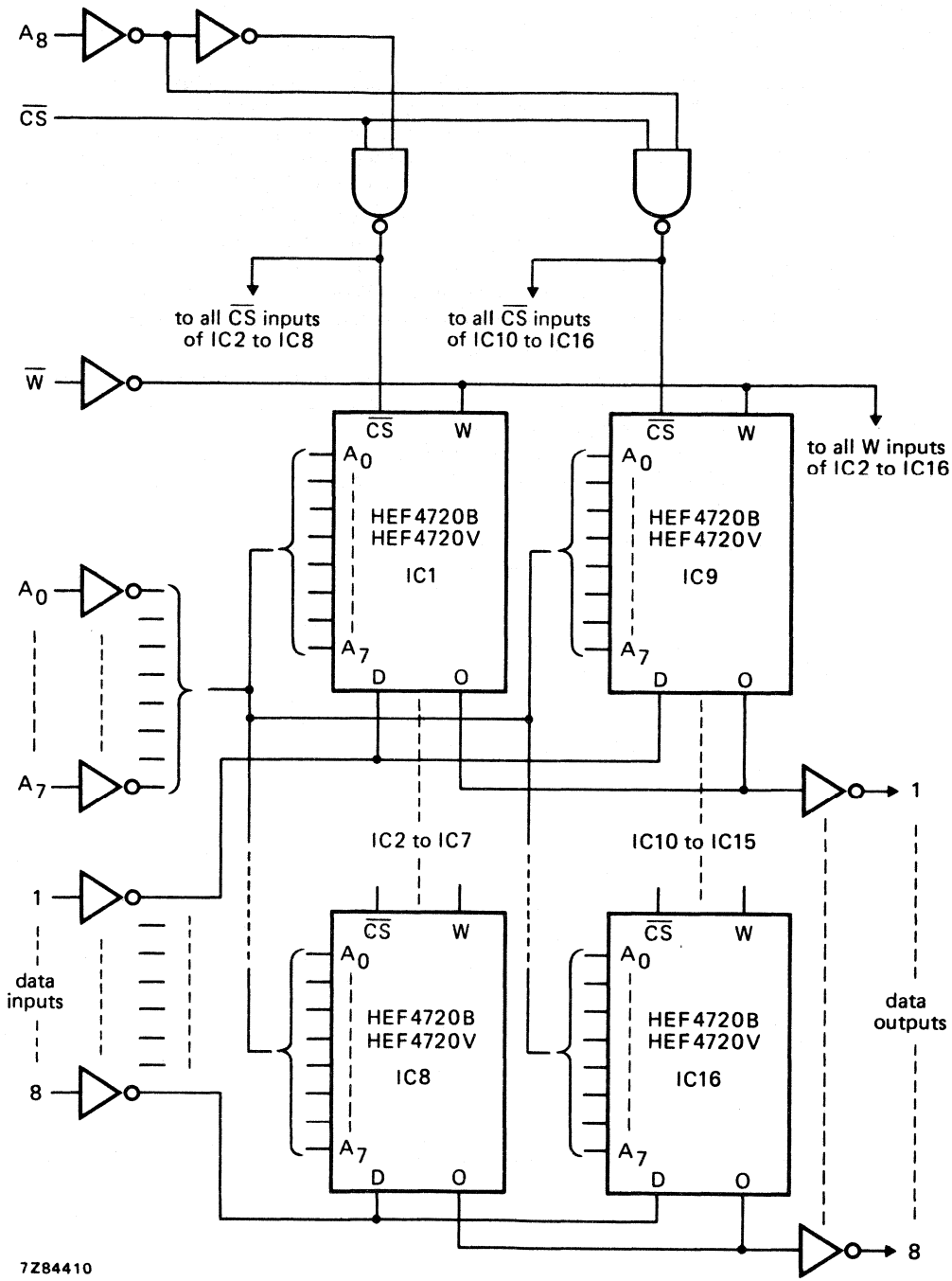


Fig. 8 Using extra HEF4720B; V ICs to obtain more words and greater word length.

APPLICATION INFORMATION (continued)

Memory retention

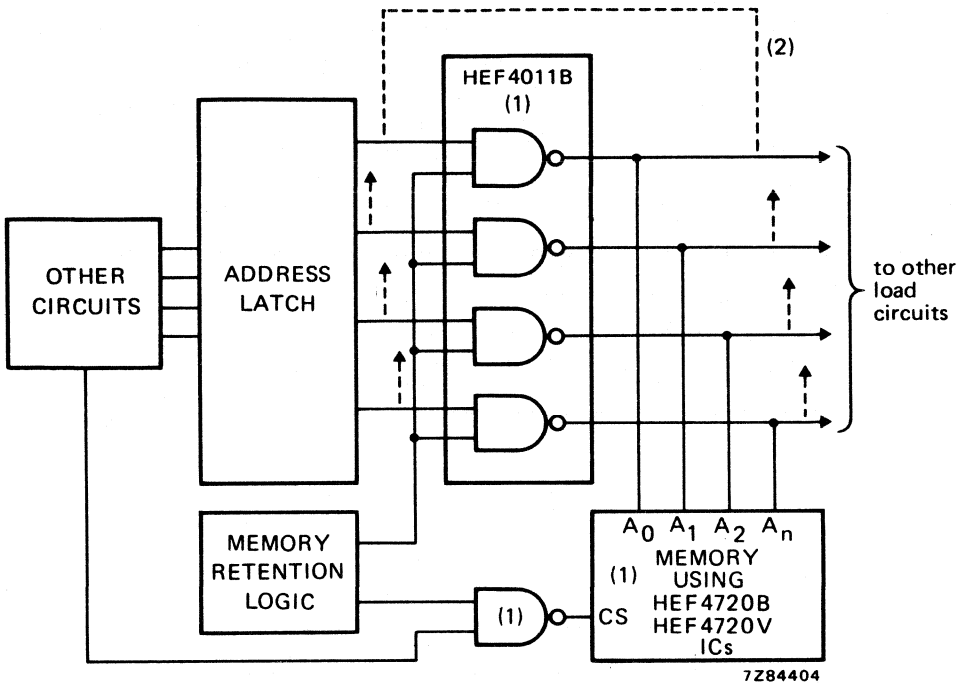
It is sometimes necessary to ensure that the information stored in the memory cannot be erased inadvertently. This can be arranged by adding detection circuits, by measures in the timing, and by the addition of a battery. With the HEF4720B; V, memory retention is very easily obtained because its current drain in the stand-by condition is almost zero. The wide supply voltage range makes it possible to keep the memory active by means of a simple battery, thereby preventing information loss.

In designing the memory retention circuits, two aspects should be kept in mind. The memory retention will not function in an optimum way if the battery voltage is low or if the voltage transitions at the address input are too slow. The first of these is usually the result of using too simple a battery back-up circuit, e.g. a battery charged via a diode from the TTL supply voltage. In this case, the LOCMOS supply voltage falls below the safe operating voltage. Special arrangements should be made to overcome this.

Slow address transitions (the second cause of memory loss) are due to a long RC-time in the power system. When the power is switched on or off, the 5 V line changes between 0 and 5 V in milliseconds to seconds so producing a correspondingly long transition time in the various logic outputs. This creates problems in the proper operation of the HEF4720B; V, with loss of memory as a possible result. This can be prevented by ensuring that input rise and fall times do not exceed 10 μs.

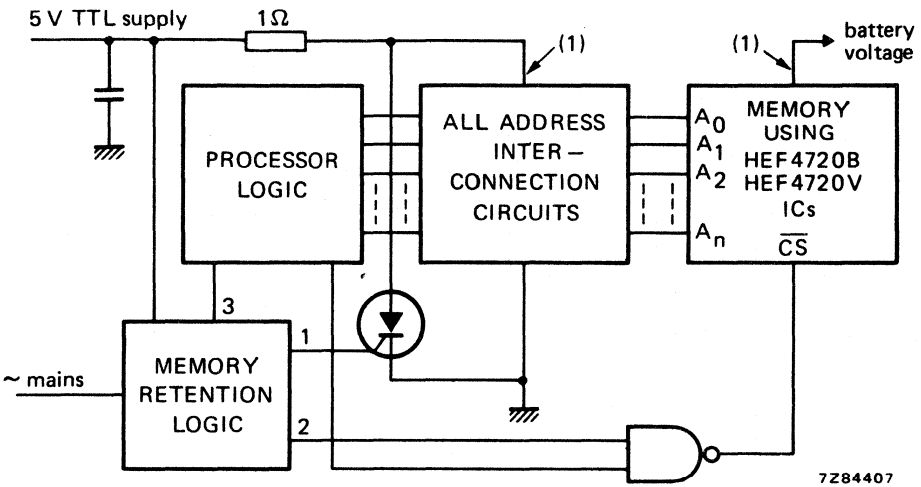
Three possibilities for controlling the rise and fall times at the HEF4720B; V interface are given here:

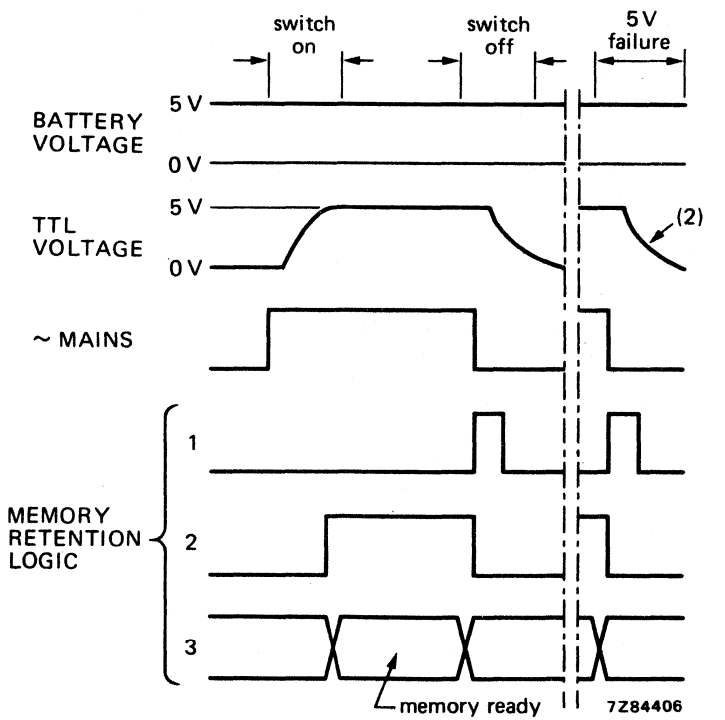
1. LOCMOS gates can be connected between the address latch and the HEF4720B; V (Fig. 9). In the event of a low voltage, or mains supply failure, the gates can be blocked by a signal from the memory retention logic thus isolating the HEF4720B; V from the address and $\overline{CS}$ inputs.
2. The interface power supply can be separated from the TTL power supply by means of a low-value resistor (Fig. 10); a thyristor is connected from the interface power supply to earth. The system is arranged so that, upon switching off or failure of the interface supply, the thyristor turns on thus ensuring a rapid fall of the supply voltage.
3. The best solution is to select the interface circuits from the LOCMOS family and to feed all these circuits from the battery (Fig. 11). These stages then remain active when the TTL 5 V supply fails. The interface circuits are mostly only active on a clock pulse, have the possibility of being inactive on a gate level, or can be forced into one position.



(1) These devices have a battery supply.
(2) Alternative connection.

Fig. 9 Use of battery-operated LOCMOS gates to isolate the memory in case of power supply failure. Devices marked (1) are connected to the battery. The HEF4011B can sink about 0,7 mA: if the load is greater than this, only the memory should be connected, other loads being connected to the address latch as shown by the dashed-line connections.





(1) Leads should be so arranged to prevent cross-talk; thyristor connections must be short.
(2) Slope > 500 mV/μs in the vicinity of the threshold.

Fig. 10 Using a thyristor to ensure a rapid fall of interface supply at switch-off or supply failure.

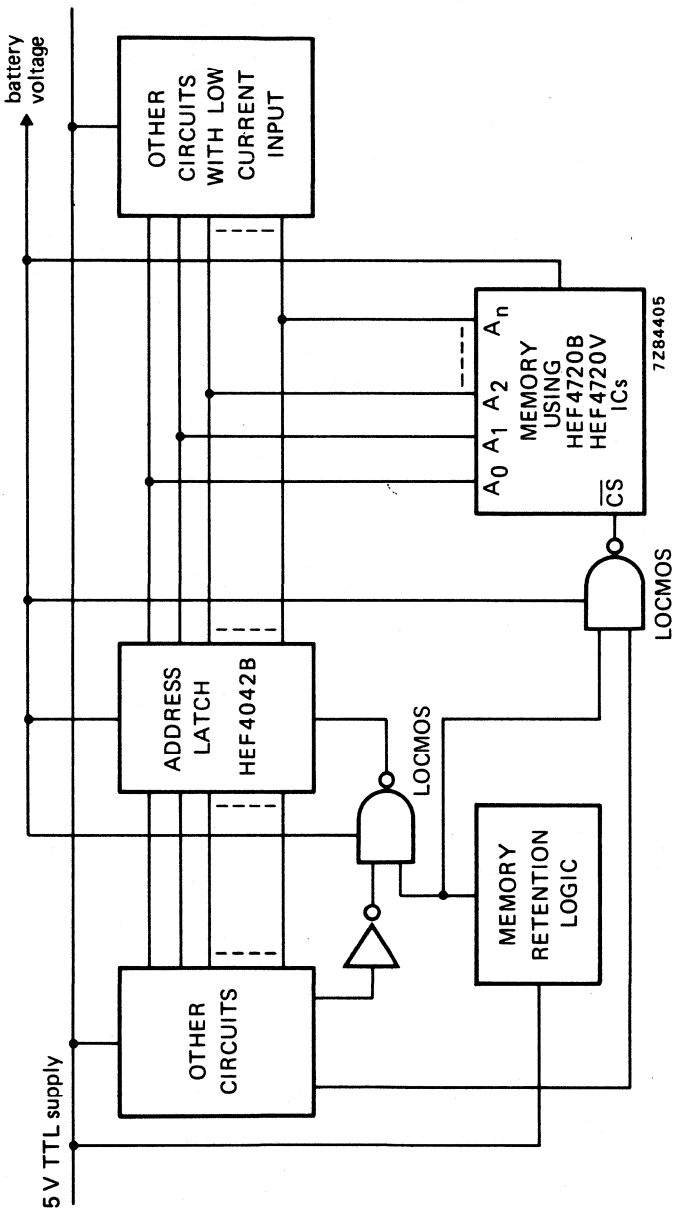


Fig. 11 Preferred solution for memory retention; all interface circuits are battery-fed LOCMOS. Note that maximum sink current of the HEF4042B is about 1,5 mA.

2048 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The SBB6116 is a 16 384-bit static random access memory organized as 2048 words of 8 bits each. A common 8-bit input/output interface is controlled by the output enable ($\overline{OE}$). A low power/standby mode, controlled by the chip select input ($\overline{CS}$), is available for memory expansion. The device operates from a 5 V power supply and is available in a 120 ns access time version. Pin compatibility with EPROM type 2716 allows a wide range of applications in microprocessor peripheral memory design.

Fabrication of this MOS device is by ion implanted complementary silicon gate technology and a process which creates high-ohmic resistors in the memory cell array (CMOS double-poly process).

Features

- Pin-compatible with EPROM type 2716
- Operating supply voltage 5 V
- Inputs protected against static charge
- Static operation requiring no clock or timing strobe
- Low power CMOS: 100 μW (typ.) standby power; 100 mW (typ.) active power
- Address activated: power consumption depends on amount of access
- Easy memory expansion
- Common data input/output interface
- All inputs and outputs directly TTL compatible
- Three-state outputs with wired-OR capability
- Output buffer control

Maximum access time

SBB6116-12: 120 ns

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

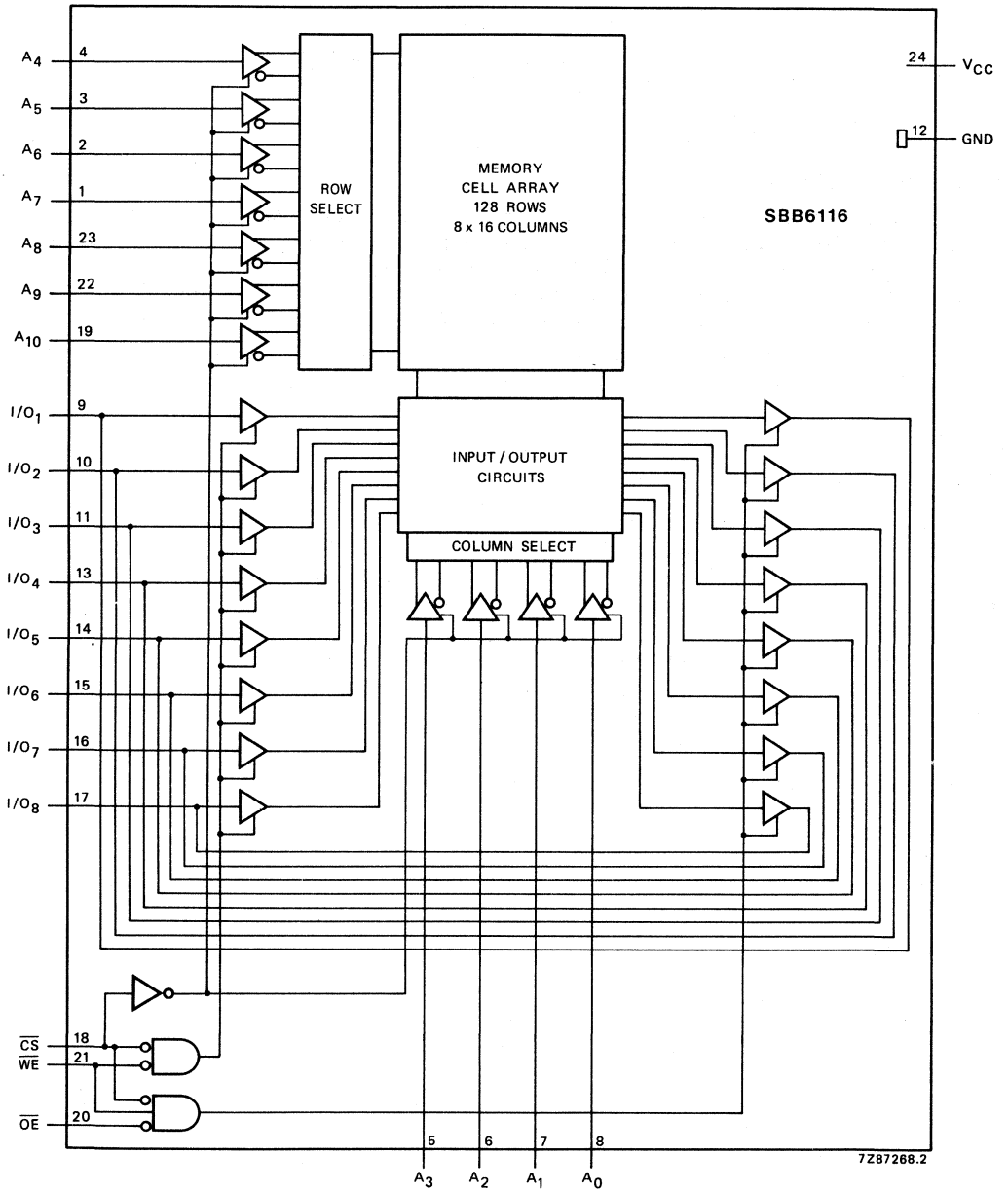


Fig. 1 Block diagram.

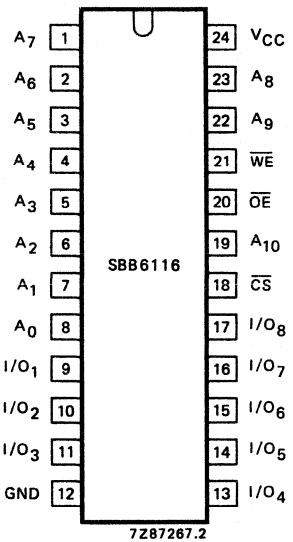


Fig. 2 Pinning diagram.

PINNING

A_0 to A_{10}	address inputs
$\overline{CS}$	chip select input
$\overline{WE}$	write enable input
I/O_1 to I/O_8	data input/output
$\overline{OE}$	output enable input
V_{CC}	positive supply (+ 5 V)
GND	negative supply (ground)

DEVELOPMENT DATA

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	mode	V_{CC} current	I/O pin	R/W cycle
H	X	X	not selected	I_{SB}, I_{SB1}	Z	
L	L	H	read	I_{CC}	D_O	read cycles 1 to 3
L	H	L	write	I_{CC}	D_I	write cycle 1
L	L	L	write	I_{CC}	D_I	write cycle 2
L	H	H	ready to read; output disbaled	I_{CC}	Z	

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

DECOUPLING REQUIREMENTS

The SBB6116 static RAM is an address-activated circuit. When an address change occurs, the precharge operation is executed by an internal pulse generated from the address transient. The consequent peak current flow following an address or $\overline{CS}$ change can induce noise on the V_{CC}/GND lines (see Fig. 3). This noise should be eliminated by the use of a 0,1 μF capacitor with good high-frequency characteristic to decouple each device. This is also important to guarantee latch-up immunity.

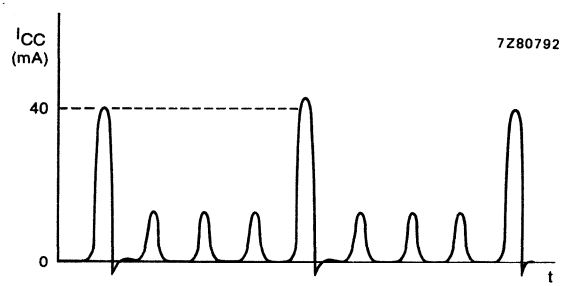


Fig. 3 Typical I_{CC} waveform with address change.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage range on any pin with respect to GND	V_I	−0,5* to + 7,0	V
Current limit for negative input voltage on any pin with respect to GND	I_I	−10	mA
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Operating temperature range with bias	T_{bias}	−10 to + 85	°C
Storage temperature range	T_{stg}	−55 to + 125	°C
Total power dissipation	P_{tot}	1,0	W

* V_{IL} = −1 V with a maximum pulse duration of 50 ns.

DEVELOPMENT DATA

RECOMMENDED D.C. OPERATING CONDITIONS

T_{amb} = 0 to + 70 °C; voltages are referenced to GND (0 V)

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	4,5	5,0	5,5	V
Input voltage HIGH	V_{IH}	2,0	3,5	6,0	V
Input voltage LOW	V_{IL}	−0,3*	–	0,8	V

D.C. CHARACTERISTICS

V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C; voltages are referenced to GND (0 V); unless otherwise specified

parameter	symbol	min.	typ.**	max.	unit
Input leakage current at V_{CC} = 5,5 V; V_I = GND to V_{CC}	$\|I_{LI}\|$	–	–	2,0	μA
Output leakage current at $\overline{CS}$ or $\overline{OE}$ = V_{IH}; $V_{I/O}$ = GND to V_{CC}	$\|I_{LO}\|$	–	–	2,0	μA
Operating power supply current at $\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA (d.c.)	I_{CC}	–	2,0	5,0	mA
Average operating current; minimum cycle time; duty factor 100%; $I_{I/O}$ = 0 mA	I_{CC2}	–	20	50	mA
Standby power supply current at $\overline{CS}$ = V_{IH}	I_{SB}	–	–	2,0	mA
at $\overline{CS} \geqslant V_{CC}$ −0,2 V or $\overline{CS} \leqslant$ 0,2 V and $V_I \geqslant V_{CC}$ −0,2 V or $V_I \leqslant$ 0,2 V	I_{SB1}	–	0,02	2,0	mA
Output voltage LOW at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = −1,0 mA	V_{OH}	2,4	–	–	V

CAPACITANCE

f = 1 MHz; T_{amb} = 25 °C

parameter	symbol	typ.	max.	unit
Input capacitance at V_I = 0 V	C_I	3	6	pF
Input/output capacitance at $V_{I/O}$ = 0 V	$C_{I/O}$	5	8	pF

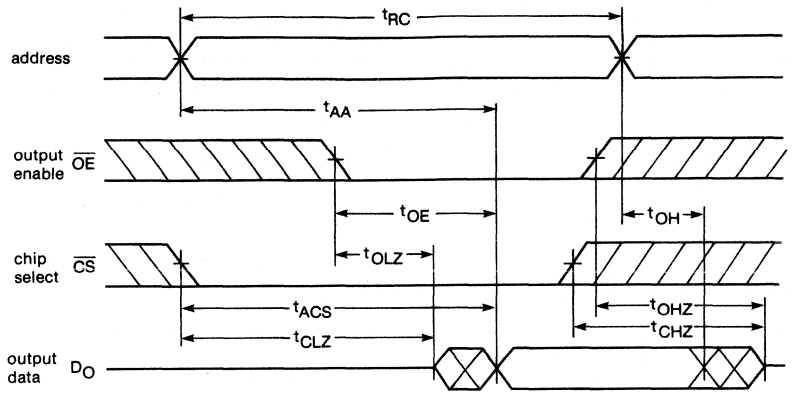
* V_{IL} = −1 V with a maximum pulse duration of 50 ns.

** At V_{CC} = 5 V; T_{amb} = 25 °C.
Typical values are given for information only.

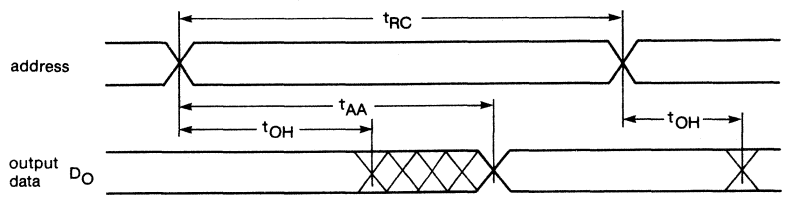
A.C. CHARACTERISTICS (Figs 4 and 5)

V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C; input pulse levels = 0,4 to 2,4 V; input rise and fall times = 5 ns; input timing reference levels = 1,5 V; output timing reference levels = 0,6 and 2,2 V; output load = 1 TTL gate and capacitance (C_L) = 100 pF (including oscilloscope and jig).

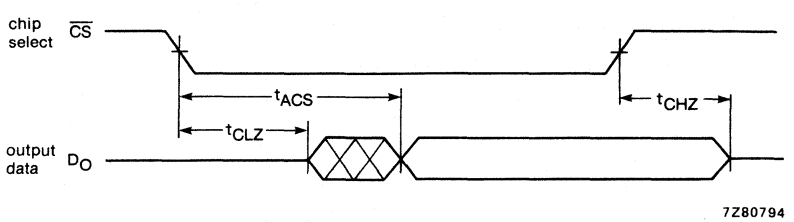
parameter	symbol	6116-12		unit
		min.	max.	
Read cycle				
Read cycle time	t_{RC}	120	–	ns
Address access time	t_{AA}	–	120	ns
Chip select access time	t_{ACS}	–	120	ns
Chip select to output in low impedance state	t_{CLZ}	10	–	ns
Output enable to output valid	t_{OE}	–	55	ns
Output enable to output in low impedance state	t_{OLZ}	10	–	ns
Output to output in high impedance state	t_{CHZ}	0	40	ns
Chip disable to output in high impedance state	t_{OHZ}	0	40	ns
Output hold from address change	t_{OH}	5	–	ns
Write cycle				
Write cycle time	t_{WC}	120	–	ns
Chip select to end of write	t_{CW}	100	–	ns
Address valid to end of write	t_{AW}	105	–	ns
Address set-up time	t_{AS}	20	–	ns
Write pulse width	t_{WP}	85	–	ns
Write recovery time	t_{WR}	0	–	ns
Output disable to output in high impedance state	t_{OHZ}	0	40	ns
Write to output in high impedance state	t_{WHZ}	0	40	ns
Data-to-write time overlap	t_{DW}	35	–	ns
Data hold from write time	t_{DH}	5	–	ns
Output active from end of write	t_{OW}	5	–	ns



(a) Read cycle 1

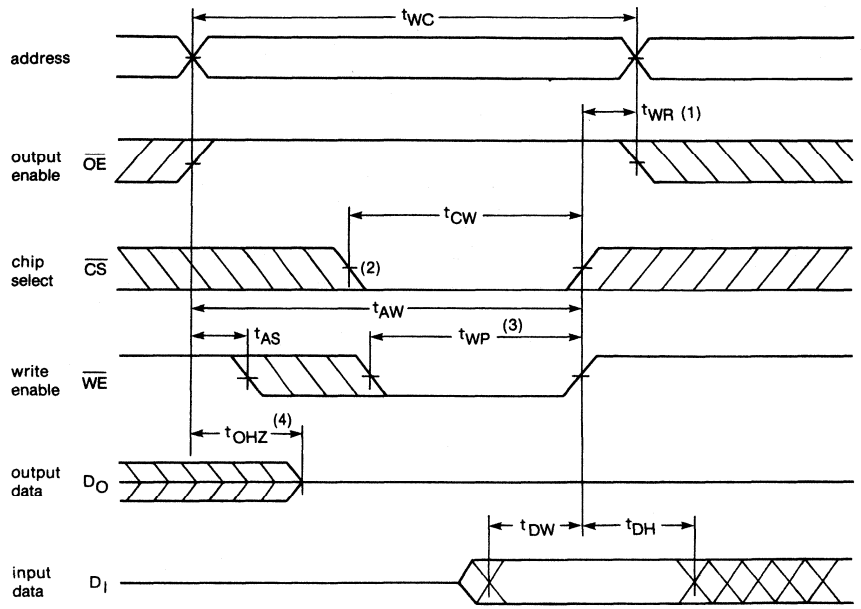


(b) Read cycle 2: device is continuously selected ($\overline{CS} = V_{IL}$); $\overline{OE} = V_{IL}$

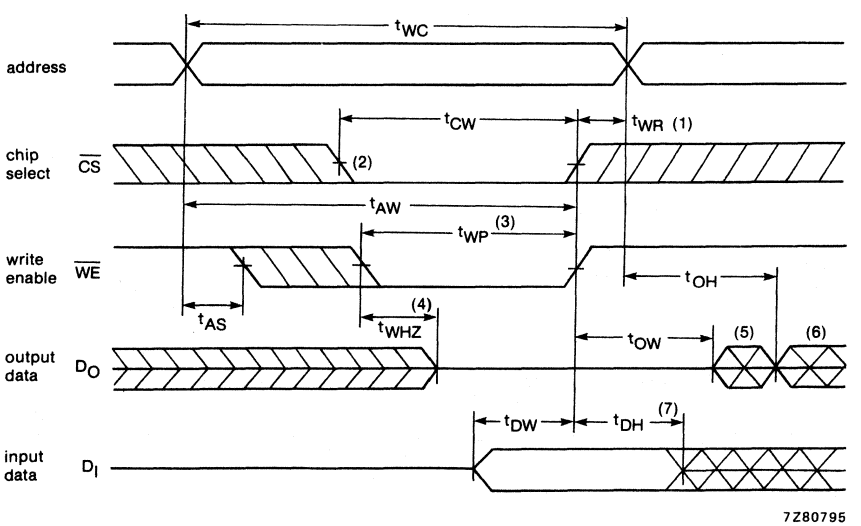


(c) Read cycle 3: address valid prior to or coincident with $\overline{CS}$ transition LOW; $\overline{OE} = V_{IL}$

Fig. 4 Read cycle timing: $\overline{WE}$ is HIGH for a read cycle; when $\overline{CS}$ is LOW the address input must not be left floating.



(a) Write cycle 1



(b) Write cycle 2: $\overline{OE} = V_{IL}$

Fig. 5 Write cycle timing: $\overline{WE}$ must be HIGH during all address transitions.

Notes to Fig. 5

1. t_{WR} is measured from $\overline{CS}$ or $\overline{WE}$ transition HIGH, whichever is the earlier, to the address change.
2. t_{WHZ} is measured under the condition CS = LOW.
3. A write occurs during the overlap (t_{WP}) of $\overline{CS}$ = LOW and $\overline{WE}$ = LOW.
4. During this period, I/O pins are in the output state and input signals of the opposite phase to the outputs must not be applied.
5. D_O has the same phase as write data of this write cycle.
6. D_O is the read data of the next address.
7. If $\overline{CS}$ is LOW during this period, I/O pins are in the output state and input signals of the opposite phase to the outputs must not be applied.

CMOS EEPROM

256 × 8-bit STATIC CMOS EEPROM WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C bus, an eight pin DIL package is sufficient. Up to eight PCF8582 devices may be connected to the I²C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572

PACKAGE OUTLINE

PCF8582P: 8-lead DIL; plastic (SOT-97).

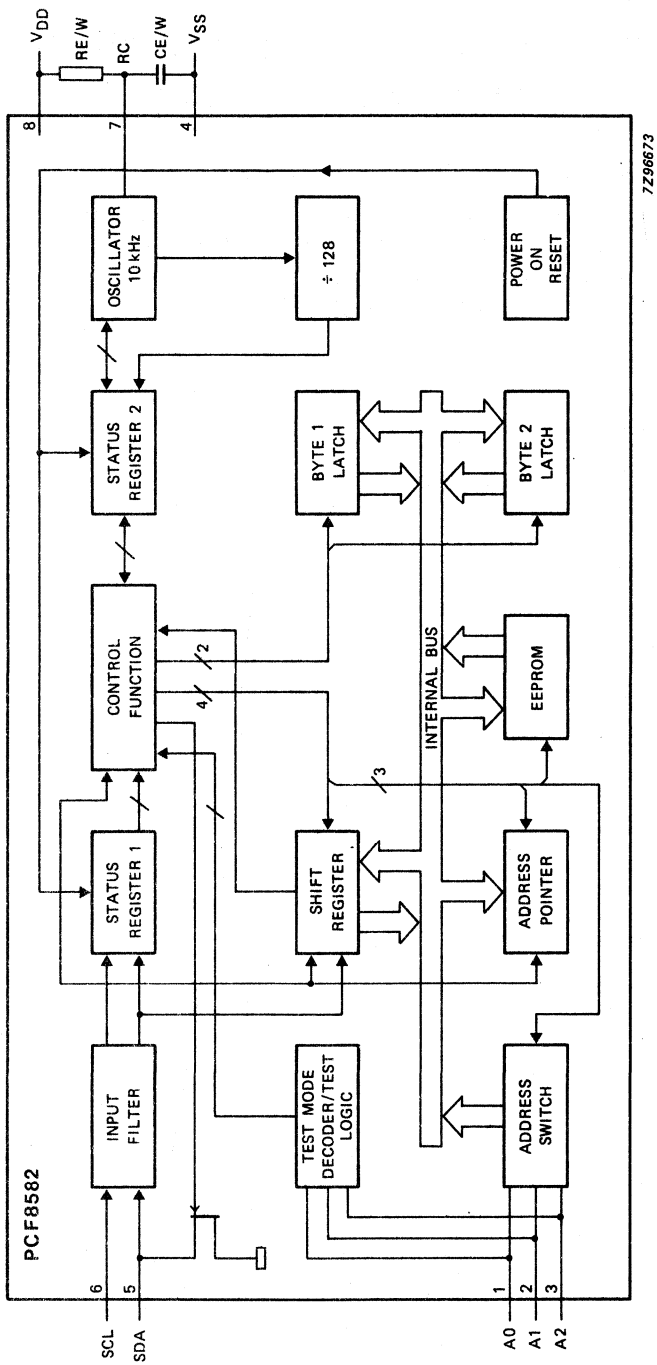


Fig. 1 Block diagram.

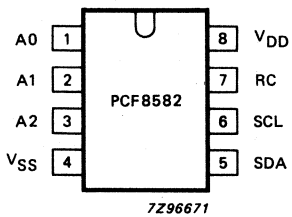


Fig. 2 Pinning diagram.

1 A0
2 A1 address inputs/test
3 A2 mode select
4 V_{SS} ground
5 SDA } I²C bus lines
6 SCL }
7 RC input for timer constant
8 V_{DD} positive supply

FUNCTIONAL DESCRIPTION

Characteristics of the I²C bus

The I²C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transfered between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCF8582 operates in both modes.
By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.
Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

The general characteristics and detailed specification of the I²C bus is available on request.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCF8582 are shown in Fig. 3.

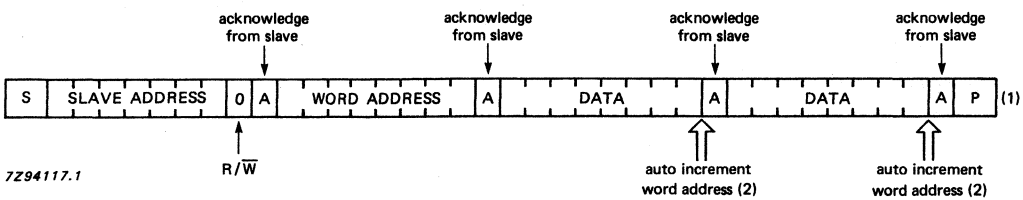


Fig. 3(a) Slave receiver ERASE/WRITE mode.

(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximatly 30 ms if only one byte is written, and 60 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two bytes.

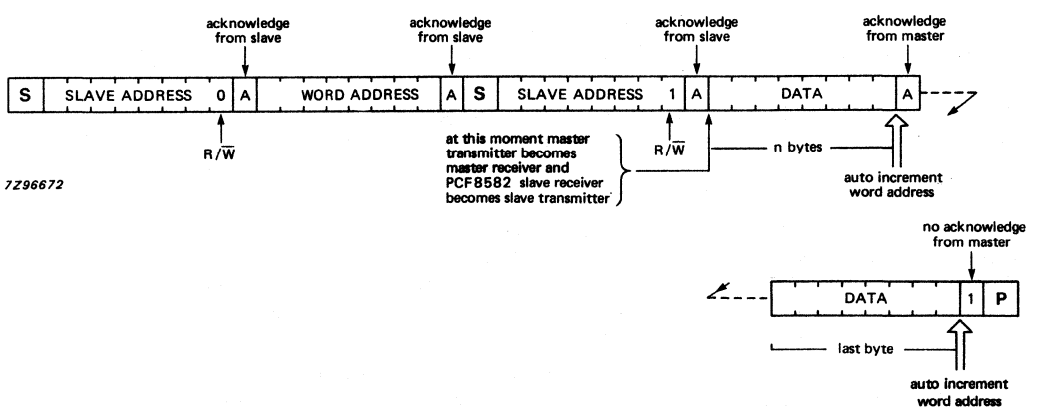


Fig. 3(b) Master reads PCF8582 slave after setting word address.
(WRITE word address; READ data).

Note: The slave address is defined in accordance with the I²C bus specification as:

1	0	1	0	A2	A1	A0	R/$\overline{W}$

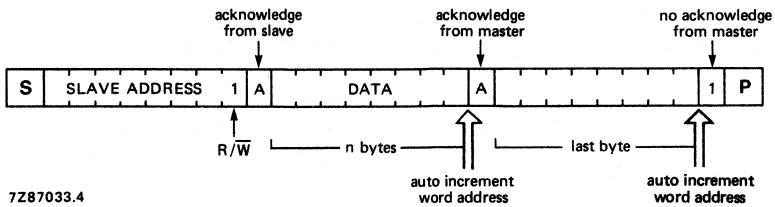


Fig. 3(c) Master reads PCF8582 slave immediately after first byte (READ mode).

I²C bus timing

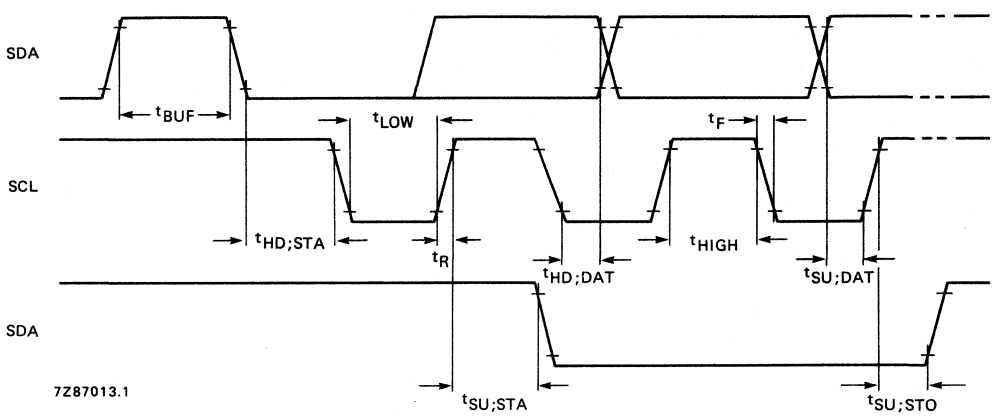


Fig. 4 I²C bus timing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 7 V
Voltage, on any input pin (input impedance 500 Ω)	V_I	V_{SS}−0,8 to V_{DD} +0,8 V
Operating temperature range	T_{amb}	−40 to +85 °C
Storage temperature range	T_{stg}	−65 to +150 °C
Current into any input pin	I_I	1 mA
Output current	I_O	10 mA

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ (f_{SCL} = 100 kHz; $V_{DD\ max}$)	I_{DDR}	–	–	0,4	mA
Operating supply current, WRITE/ERASE($V_{DD\ max}$)	I_{DDW}	–	–	2,0	mA
Standby supply current ($V_{DD\ max}$)	I_{DDO}	–	–	10	μA
Input SCL and input/output SDA					
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input voltage HIGH	V_{IH}	3	–	V_{DD}+0,8	V
Output voltage LOW (I_{OL} = 3 mA, V_{DD} = 4,5 V)	V_{OL}	–	–	0,4	V
Output leakage current HIGH (V_{OH} = V_{DD})	I_{OH}	–	–	1	μA
Input leakage current (A0,A1,A2,SCL), (note 1)	$\pm I_{IN}$	–	–	1	μA
Clock frequency	f_{SCL}	0	–	100	kHz
Input capacity (SCL,SDA)	C_I	–	–	7	pF
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
Set-up time for start condition (only relevent for a repeated start condition)	$t_{SU;STA}$	4,7	–	–	μs
Hold time DATA for:					
I^2C bus compatible masters	$t_{HD;DAT}$	5	–	–	μs
I^2C devices (note 2)	$t_{HD;DAT}$	200	–	–	ns
Set-up time DATA	$t_{SU;DAT}$	500	–	–	ns
Rise time for both SDA and SCL lines	t_R	–	–	1	μs
Fall time for both SDA and SCL lines	t_F	–	–	300	ns
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	–	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms (± 10% tolerance)	$C_{E/W}$	–	3,3	–	nF
Erase/write timing resistor for erase/write cycle of 30 ms (± 5% tolerance)	$R_{E/W}$	–	56	–	kΩ
Data retention time (T_{amb} = +55 °C)	t_S	10	–	–	years

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

CMOS EPROM

27C64A/87C64
64K (8K X 8) CMOS UV Erasable PROM

Preliminary Specification

FEATURES

- **CMOS microcontroller and microprocessor compatible**
  - **87C64-Integrated address latch**
  - **Universal 28-Pin memory site, 2-line control**
- **Low power consumption**
  - **10mA maximum CMOS active current**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through Epitaxial processing**
- **Fast, reliable intelligent programming**
  - **Programs in under 1 minute**
  - **12.5V V_{PP}**

DESCRIPTION

Signetics 27C64A and 87C64 CMOS EPROMs are 64K-bit 5V only memories organized as 8192 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 87C64 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C64A has a non-multiplexed addressing interface and is plug compatible with the industry standard 2764.

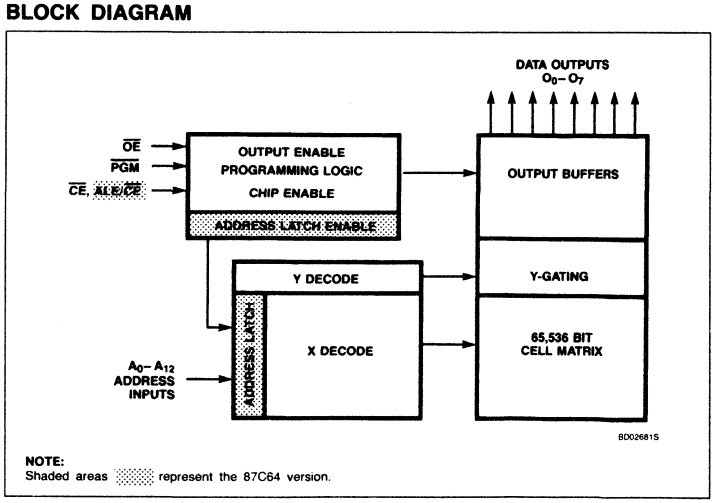
The 27C64A and 87C64 achieve both high-performance (200ns access times) and low power consumption (10mA active current maximum, CMOS inputs) making them ideal for high-performance, portable equipment.

The highest degree of protection against latch-up is achieved through Epitaxial processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins from −1V to V_{CC} +1V.

The 87C64 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can tie combined (multiplexed) address-data processor busses directly into both the $A_0 - A_7$ and O_0-O_7 pins of the 87C64. During ALE high (ALE/$\overline{CE}$) the address information is allowed to flow into the EPROM and begin accessing the stored code. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs is latched internally. The $A_0 - A_7$ inputs are then ignored as data information is passed on the same bus from the EPROM $O_0 - O_7$ pins (ALE/$\overline{CE}$ remains low).

The 27C64A and 87C64 are offered in ceramic DIP packages. Both devices can be programmed with standard EPROM Programmers and the intelligent programming algorithm may be utilized.

BLOCK DIAGRAM



NOTE:
Shaded areas ▒▒ represent the 87C64 version.

PIN CONFIGURATION

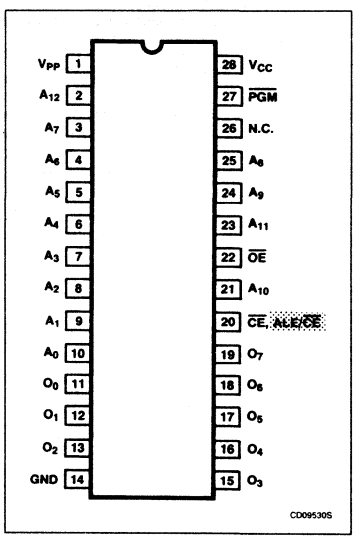


Table 1. Pin Names

$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
ALE/$\overline{CE}$	Address latch enable/chip enable
$\overline{PGM}$	Program strobe
N.C.	No connect
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

ORDERING INFORMATION

DESCRIPTION	VOLTAGE RANGE	ORDER CODE[1]
27C64A-20	V_{CC} ±10%	27C64A-20FA
27C64A-25	V_{CC} ±10%	27C64A-25FA
27C64A-30	V_{CC} ±10%	27C64A-30FA
87C64-20	V_{CC} ±10%	87C64-20FA
87C64-25	V_{CC} ±10%	87C64-25FA
87C64-30	V_{CC} ±10%	87C64-30FA

NOTE:
1. All packages are 28-pin cerdips with quartz windows.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Temperature under bias	−10 to +80	°C
Storage temperature	−65 to +125	°C
Voltage on any pin with respect to ground	−2.0 to V_{CC}+1V[1]	V
Voltage on pin-24 with respect to ground	−2.0 to +13.5[1]	V
V_{PP} supply voltage with respect to ground during programming	−2.0 to +14.0[1]	V
Operating temperature during read	0 to +70[2]	°C

NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION DC CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	NOTES
			Min	Typ[3]	Max		
I_{LI}	Input leakage current	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA	
I_{LO}	Output leakage current	$V_{OUT} = 5.5V = V_{CC}$		0.01	1.0	µA	
I_{CC} TTL	Operating current TTL inputs	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$, $O_{0-7} = 0mA$			20, 30	mA	4, 6
I_{CC} CMOS	Operating current	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$, $O_{0-7} = 0mA$			10	mA	4, 6
I_{SB} TTL	Standby current TTL inputs	$\overline{CE} = V_{IH}$			1.0	mA	4
I_{SB} CMOS	Standby current CMOS inputs	$\overline{CE} = V_{IH}$			100.0	µA	5
I_{PP}	V_{PP} read current	$V_{PP} = V_{CC}$			100.0	µA	6
V_{IL}	Input low voltage (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V	
	Input low voltage (CMOS)		-0.2		0.2		
V_{IH}	Input high voltage	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V	
	Input high voltage (CMOS)		$V_{CC} - 0.2$		$V_{CC} + 0.2$		
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V	
V_{OH}	Output high voltage	$I_{OH} = -2.5mA$	3.5			V	
I_{OS}	Output short circuit current				100	mA	7
V_{PP}	V_{PP} read voltage		$V_{CC} - 0.7$		V_{CC}	V	8

NOTES:
1. Minimum DC input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
2. Operating temperature is for commercial product defined by this specification.
3. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$.
4. 30mA for -20 version, 20mA for -25 and -30 versions.
   TTL inputs: spec V_{IL}, V_{IH} levels
   CMOS inputs: GND ± 0.2 to $V_{CC} \pm 0.2$
5. ALE/$\overline{CE}$ or $\overline{CE}$ is $V_{CC} \pm 0.2V$. All other inputs can have any value within spec.
6. Maximum Active power usage is the sum $I_{PP} + I_{CC}$.
7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

CAPACITANCE[1] T_A = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	CONDITIONS	MAX	UNIT
C_{IN}	Address/control capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	12	pF

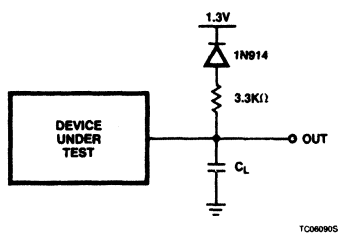
NOTE:
1. Sampled. Not 100% tested.

Table 2. Read Modes for 27C64A/87C64

MODE	PINS				
	ALE/$\overline{CE}$ $\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	OUTPUTS (11 - 13, 15 - 19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z

NOTE:
X can be V_{IH} or V_{IL}.

AC TESTING LOAD CIRCUIT



NOTES:
C_L = 100pF
C_L Includes Jig Capacitance

Figure 1. Test Configuration

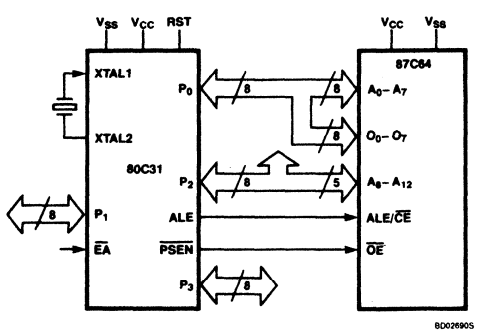


Figure 2. 80C31 with 87C64 System Configuration

READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

READ MODE: 87C64

The 87C64 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C64 is designed as shown in Figure 2. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C64. A separate address latch is eliminated.

The 87C64 internal address latch is directly enabled through the use of the ALE/$\overline{CE}$ line. As the transition occurs on the ALE/$\overline{CE}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM via the $\overline{OE}$ pin.

STANDBY MODE

The 27C64A and 87C64 have Standby modes which reduce the maximum V_{CC} current to 100μA. Both are placed in the Standby mode when pin 20 is in the high state. When in the Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

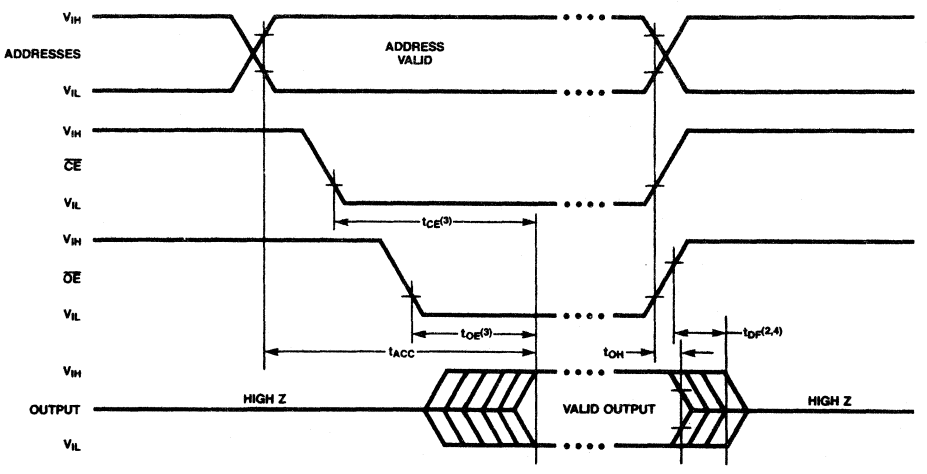
READ OPERATION

AC CHARACTERISTICS: 27C64A[1] $0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

VERSIONS		27C64A-20		27C64A-25		27C64A-30		UNIT
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to output delay		200		250		300	ns
t_{OE}	$\overline{OE}$ to output delay		75		100		120	ns
t_{DF}[2]	$\overline{OE}$ or $\overline{CE}$ high to output high Z		55		60		75	ns
t_{OH}[2]	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first	0		0		0		ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.

AC WAVEFORMS: 27C64A



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

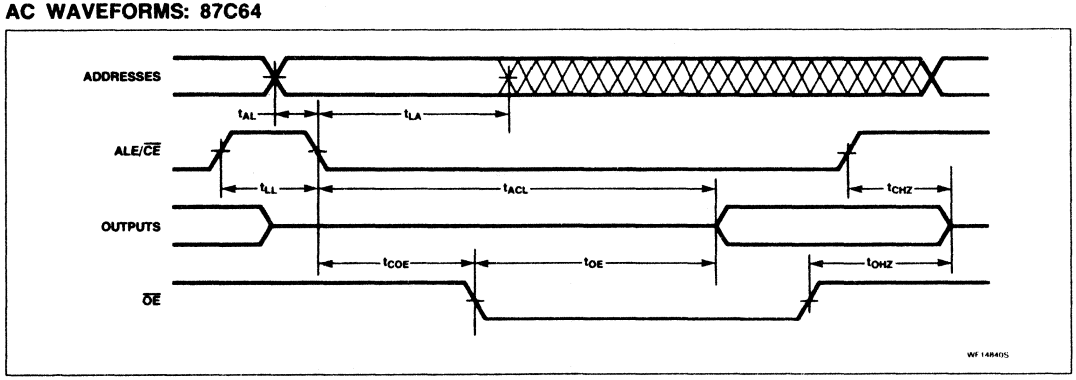
READ OPERATION

AC CHARACTERISTICS: 87C64[1] $0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

VERSIONS		87C64-20		87C64-25		87C64-30		UNIT
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{LL}	Chip deselect width	50		60		75		ns
t_{AL}	Address to $\overline{CE}$ - latch setup	20		25		30		ns
t_{LA}	Address hold from $\overline{CE}$ - LATCH	45		50		60		ns
t_{ACL}	$\overline{CE}$ - latch access time		200		250		300	ns
t_{OE}	Output enable to output valid		75		100		120	ns
t_{COE}	$\overline{CE}$ to output enable	45		50		60		ns
t_{CHZ}[2]	Chip deselect to output in High Z		50		60		75	ns
t_{OHZ}[2]	Output disable to output in High Z		50		60		75	ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.

AC WAVEFORMS: 87C64



ERASURE CHARACTERISTICS

The erasure characteristics of the 27C64A and 87C64 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C64A or 87C64 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C64A or 87C64 are to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C64A and 87C64 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The 27C64A or 87C64 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C64A or 87C64 can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100mA and voltages from -1V to V_{CC} + 1V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

Table 3. Programming Modes for 27C64A and 87C64

MODE	PINS							
	ALE/$\overline{CE}$ $\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A_9 (24)	A_0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11 – 13, 15 – 19)
Intelligent Programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.0V[4]	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.0V[4]	D_{OUT}
Program inhibit	V_{IH}	X	X	X	X	V_{PP}	6.0V[4]	HIGH Z
Intelligent identifier[3] –Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{CC}	V_{CC}	15 H
Intelligent identifier[3] –27C64A	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IH}	V_{CC}	V_{CC}	OB H
Intelligent identifier[3] –87C64	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IH}	V_{CC}	V_{CC}	37 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. $A_1 - A_8$, $A_{10-12} = V_{IL}$
4. $V_{CC} = 6.0V \pm 0.25V$

PROGRAMMING

Caution: Exceeding 14.0V on Pin 1 (V_{PP}) may permanently damage the 27C64A or 87C64.

Initially, and after each erasure, all bits of the 27C64A or 87C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27C64A or 87C64 are in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C64A and 87C64 intelligent programming algorithms rapidly program CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of one minute. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27C64A or 87C64 intelligent program algorithm is shown in Figure 3.

The Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is an iteration counter and is equal to the number of the initial 1ms pulses applied to a particular 27C64A or 87C64 location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0V$ and $V_{PP} = 12.5V$.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = 5.0V$.

PROGRAM INHIBIT

Programming of multiple 27C64A or 87C64 EPROMs in parallel with different data is easily accomplished by using the program inhibit mode. A high-level $\overline{CE}$ or ALE/$\overline{CE}$ input inhibits other 27C64A or 87C64 EPROMs from being programmed.

Except for $\overline{CE}$ or ALE/$\overline{CE}$ all inputs of the parallel 27C64As or 87C64s may be common. A TTL low-level pulse applied to the $\overline{PGM}$ and $\overline{CE}$ or ALE/$\overline{CE}$ input with V_{PP} at 12.5V will program the selected 27C64A or 87C64.

VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ or ALE/$\overline{CE}$ at V_{IL}, and $\overline{PGM}$ at V_{IH}. Data should be verified a minimum of t_{OEV} after the falling edge of $\overline{OE}$.

Intelligent Identifier Mode

The intelligent identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C64A or 87C64.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the 27C64A or 87C64. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during intelligent identifier mode.

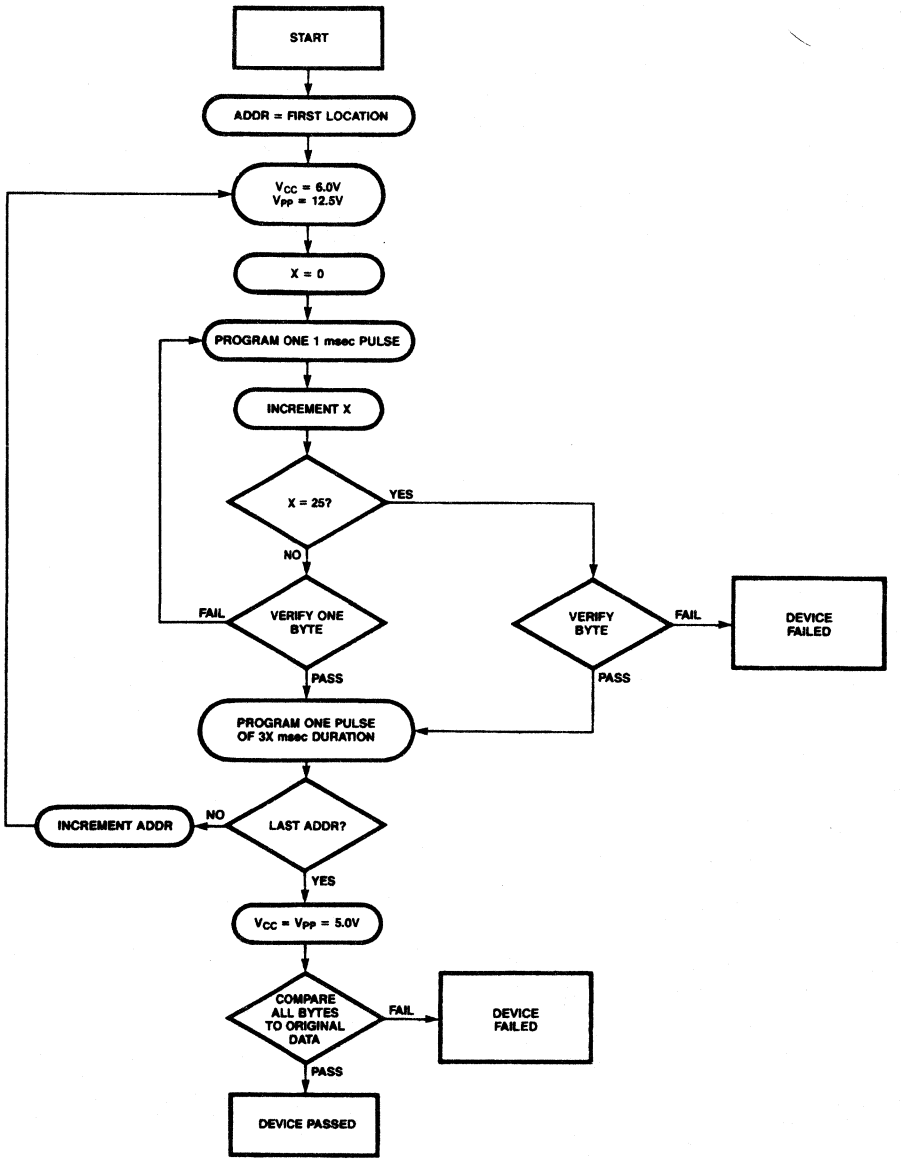


Figure 3. 27C64A and 87C64 intelligent programing Flowchart

INTELLIGENT PROGRAMMING ALGORITHM

DC PROGRAMMING CHARACTERISTICS: T_A = 25°C ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		LIMITS
			Min	Max	
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} + 0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	O_{0-7} = 0mA		30	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		30	mA

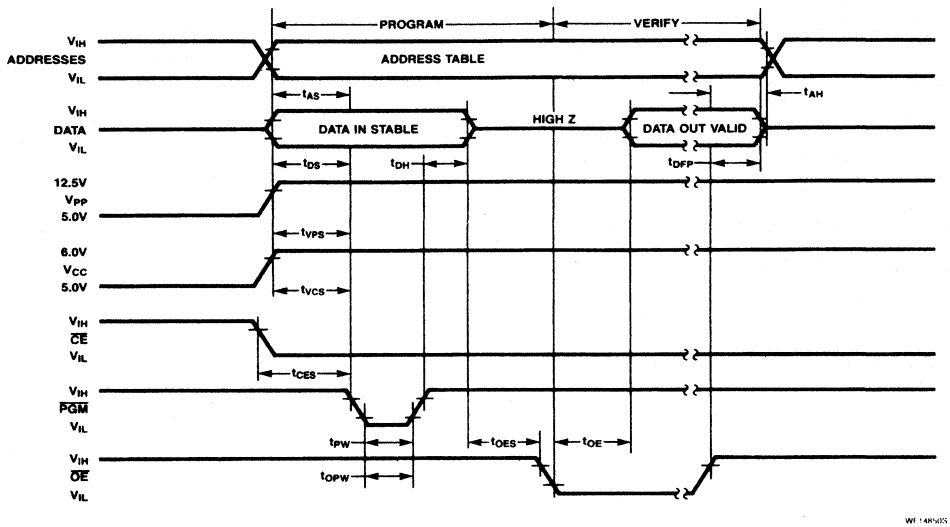
AC PROGRAMMING CHARACTERISTICS: 27C64A

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP} [3]	$\overline{OE}$ high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{PGM}$ initial program pulse width	(See Note 1)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ overprogram pulse width	(See Note 2)	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. Initial program pulse width tolerance is 1msec ± 5%.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven - see timing diagram.



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C64A, a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

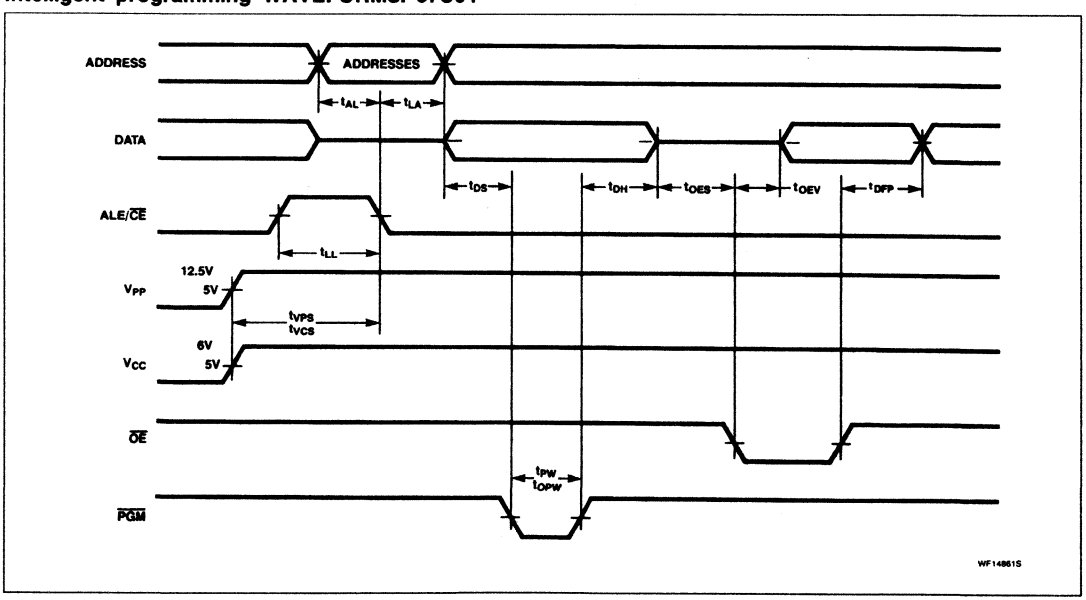
Figure 4. Intelligent programming Waveforms: 27C64A

AC PROGRAMMING CHARACTERISTICS: 87C64 T_A = 25°C ±5°C, V_{CC} = 6.0 ±2.5V, V_{PP} = 12.5V ±0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{LL}	Chip deselect width		2			µs
t_{AL}	Address to chip select setup		1			µs
t_{LA}	Address hold from chip select		1			µs
t_{PW}	$\overline{PGM}$ initial pulse width		0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{DS}	Data setup time		2			µs
t_{DFP}	$\overline{OE}$ high to data float				150	ns
t_{OES}	Output enable setup time		2			µs
t_{OEV}	Data valid from output enable				150	ns
t_{DH}	Data hold time		2			µs

NOTE:
Programming tolerances and test conditions are the same as 27C64A.

Intelligent programming WAVEFORMS: 87C64



27C256/87C256
256K (32K × 8) CMOS UV Erasable PROM

Preliminary Specification

FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **87C256-Integrated address latch**
  - **Universal 28-Pin memory site, 2-line control**
- **Low power consumption**
  - **10mA maximum CMOS active current**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **170ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V V_{PP}**

DESCRIPTION

Signetics' 27C256 and 87C256 CMOS EPROMs are 256K-bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 87C256 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C256 has a non-multiplexed addressing interface and is plug compatible with the industry standard 27256.

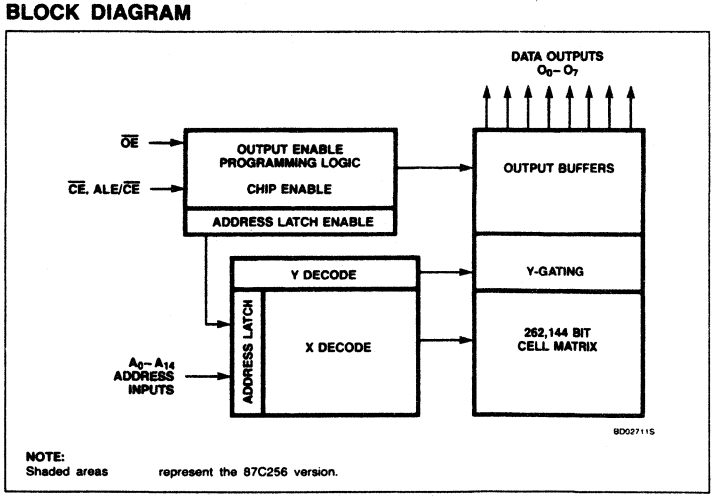
The 27C256 and 87C256 achieve both high-performance (170ns access time for 27C256) and low power consumption (10mA active current maximum, CMOS inputs) making them, ideal for high-performance, portable equipment.

The highest degree of protection against latch-up is achieved through epitaxial processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins from −1V to V_{CC} +1V.

The 87C256 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can tie combined (multiplexed) address-data processor busses directly into both the $A_0 - A_{14}$ and $O_0 - O_7$ pins of the 87C256. During ALE high (ALE/$\overline{CE}$) the address information is allowed to flow into the EPROM and begin accessing the stored code. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs is latched internally. The $A_0 - A_7$ inputs are then ignored as data information is passed on the same bus from the EPROM $O_0 - O_7$ Pins (ALE/$\overline{CE}$ remains low).

The 27C256 and 87C256 are offered in ceramic DIP Packages. Both devices can be programmed with standard EPROM Programmers and the intelligent programming algorithm may be utilized.

BLOCK DIAGRAM



NOTE:
Shaded areas represent the 87C256 version.

PIN CONFIGURATION

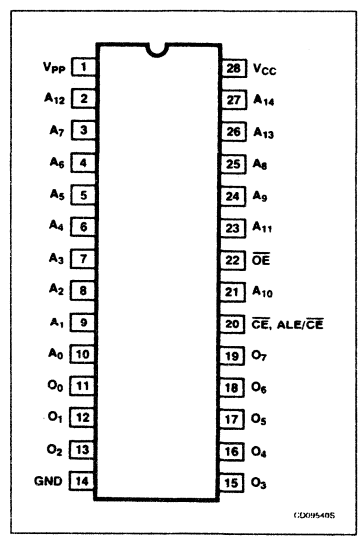


Table 1. Pin Names

$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
ALE/$\overline{CE}$	Address latch enable/chip enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

ORDERING INFORMATION

DESCRIPTION	VOLTAGE RANGE	ORDER CODE[1]
27C256-17	V_{CC} ±10%	27C256-17FA
27C256-20	V_{CC} ±10%	27C256-20FA
27C256-25	V_{CC} ±10%	27C256-25FA
27C256-30	V_{CC} ±10%	27C256-30FA
87C256-20	V_{CC} ±10%	87C256-20FA
87C256-30	V_{CC} ±10%	87C256-30FA

NOTE:
1. All packages are cerdips with quartz windows.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Temperature under bias	10 to 80	°C
Storage temperature	−65 to +125	°C
Voltage on any pin with respect to ground	−2.0 to V_{CC} +1V[1]	V
Voltage on pin 24 with respect to ground	−2.0 to +13.5[1]	V
V_{PP} supply voltage with respect to ground during programming	−2.0 to +14.0[1]	V
Operating temperature during read	0 to −70[2]	°C

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

READ OPERATION DC CHARACTERISTICS: 27C256/87C256 $0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				NOTES
			Min	Typ[3]	Max	Unit	
I_{LI}	Input leakage current	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA	
I_{LO}	Output leakage current	$V_{OUT} = 5.5V = V_{CC}$		0.01	1.0	µA	
I_{CC} TTL	Operating current TTL inputs	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			30	mA	8
I_{CC} CMOS	Operating current CMOS inputs	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			10	mA	8
I_{SB} TTL	Standby current TTL inputs	$\overline{CE} = V_{IH}$			2	mA	8
I_{SB} CMOS	Standby current CMOS inputs	$\overline{CE} = V_{IH}$			100	µA	4
I_{PP}	V_{PP} read current	$V_{PP} = V_{CC}$			200	µA	5
V_{IL}	Input low voltage (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V	
	Input low voltage (CMOS)		-0.2		0.2		
V_{IH}	Input high voltage (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V	
	Input low voltage (CMOS)		$V_{CC} - 0.2$		$V_{CC} + 0.2$		
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V	
V_{OH}	Output high voltage	$I_{OH} = -400µA$	2.4			V	
I_{OS}	Output short-circuit current				100	mA	6
V_{PP}	V_{PP} read voltage		$V_{CC} - 0.7$		V_{CC}	V	7

NOTES:
1. Minimum DC input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
2. Operating temperature is for commercial product defined by this specification.
3. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$.
4. Other inputs can have any value within spec.
5. Maximum Active power usage is the sum $I_{PP} + I_{CC}$.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
8. TTL Inputs: Spec TTL at V_{IL}, V_{IH} levels.
   CMOS Inputs: GND ±0.2V to V_{CC}±0.2V.

CAPACITANCE[1] T_A = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	CONDITIONS	MAX	UNIT
C_{IN}	Address/control capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	12	pF

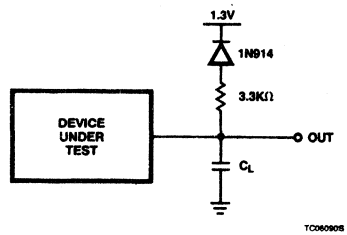
NOTE:
Sampled Not 100% tested.

Table 2. Read Modes for 27C256/87C256

MODE	PINS			
	ALE/$\overline{CE}$ $\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	OUTPUTS (11 - 13, 15 - 19)
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	High Z

NOTE:
X can be V_{IH} or V_{IL}.

AC TESTING LOAD CIRCUIT



NOTES:
1. C_L pF
2. C_L includes Jig Capacitance

Figure 1. Test Configuration

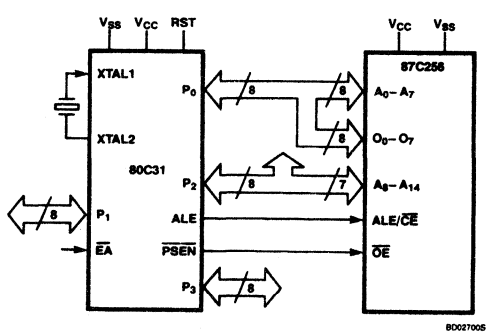


Figure 2. 80C31 with 87C256 System Configuration

READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

READ MODE: 87C256

The 87C256 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C256 is designed as shown in Figure 2. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C256. A separate address latch is eliminated.

The 87C256 internal address latch is directly enabled through the use of the ALE/$\overline{CE}$ line. As the transition occurs on the ALE/$\overline{CE}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM via the $\overline{OE}$ pin.

STANDBY MODE

The 27C256 and 87C256 have Standby modes which reduce the maximum CMOS V_{CC} current to 100μA. Both are placed in the Standby mode when pin 20 is in the high state. When in the Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

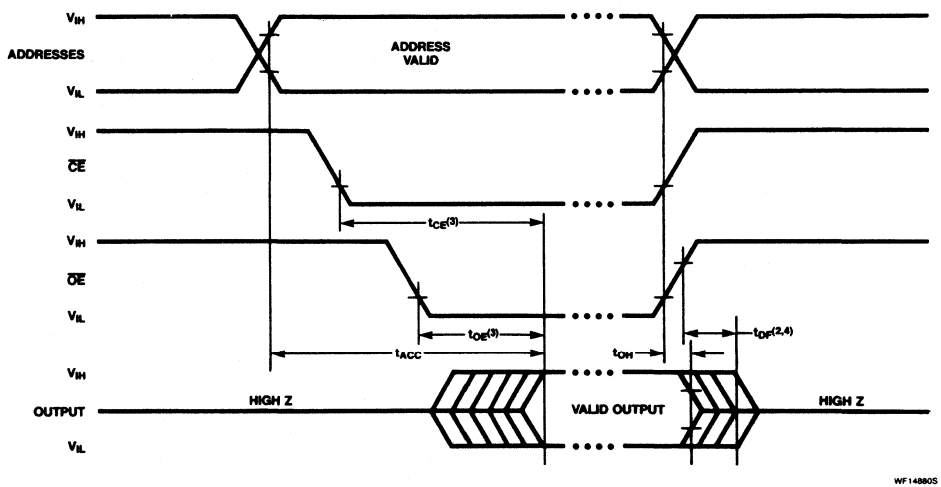
READ OPERATION

AC CHARACTERISTICS: 27C256[1] $0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

VERSIONS		27C256 - 17		27C256 - 20		27C256 - 25		27C256 - 30		UNITS
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to output delay		170		200		250		300	ns
t_{OE}	$\overline{OE}$ to output delay		70		75		100		120	ns
t_{DF}[2]	$\overline{OE}$ or $\overline{CE}$ high to output High Z		55		55		60		75	ns
t_{OH}[2]	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first	0		0		0		0		ns

NOTES:
1. AC characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.

AC WAVEFORMS: 27C256



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

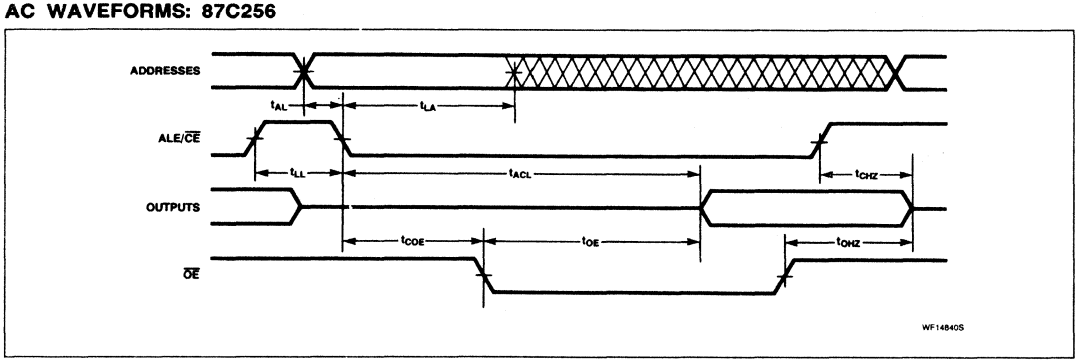
READ OPERATION

AC CHARACTERISTICS: 87C256[1] $0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

VERSIONS		87C256 - 20		27C256 - 30		UNITS
Symbol	Parameter	Min	Max	Min	Max	
t_{LL}	Chip deselect width	50		75		ns
t_{AL}	Address to $\overline{CE}$ - latch setup	20		30		ns
t_{LA}	Address hold from $\overline{CE}$ - LATCH	45		60		ns
t_{ACL}	$\overline{CE}$ - latch access time		200		300	ns
t_{OE}	Output enable to output valid		75		120	ns
t_{COE}	$\overline{CE}$ to output enable	45		60		ns
t_{CHZ}	Chip deselect to output in high Z		55		75	ns
t_{OHZ}[2]	Output disable to output in high Z		55		75	ns

NOTES:
1. AC characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.

AC WAVEFORMS: 87C256



SYSTEM CONSIDERATIONS: 27C256/87C256

The power switching characteristics of CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer — the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Two-Line Control and by properly selected decoupling capacitors.

It is recommended that a $0.1\mu F$ ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a $4.7\mu F$ bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C256 and 87C256 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C256 or 87C256 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C256 or 87C256 are to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C256 and 87C256 is exposure to short-wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a $12{,}000\mu W/cm^2$ power rating. The 27C256 or 87C256 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C256 or 87C256 can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ $12000\mu W/cm^2$). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

Table 3. Programming Modes for 27C256 and 87C256

MODE	PINS						
	ALE/$\overline{CE}$ CE (20)	$\overline{OE}$ (22)	A_0 (24)	A_9 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11 - 13, 15 - 19)
Intelligent programming	V_{IL}	V_{IH}	X	X	V_{PP}	6.0V[4]	D_{IN}
Program verify	V_{IH}	V_{IL}	X	X	V_{PP}	6.0V[4]	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	X	V_{PP}	6.0V[4]	HIGH Z
Intelligent identifier[3] -manufacturer	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	V_{CC}	15 H
Intelligent identifier[3] -27C256	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	8C H
Intelligent identifier[3, 5] -87C256	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	80 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. $A_1 - A_8$, $A_{10-12} = V_{IL}$.
4. V_{CC} = 6.0V ± 0.25V.
5. ALE/$\overline{CE}$ has to be toggled in order to latch in the addresses and read the signature codes.

CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100mA and voltages from −1V to V_{CC}+1V.

Additionally, the Vpp (programming) pin is designed to resist latch-up to the 14V maximum device limit.

PROGRAMMING

Caution: Exceeding 14.0V on pin 1 (Vpp) may permanently damage the 27C256 or 87C256.

Initially, and after each erasure, all bits of the 27C256 or 87C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27C256 or 87C256 are in the programming mode when the Vpp input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C256 and 87C256 intelligent programming intelligent algorithms rapidly program Signetic's CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27C256 or 87C256 intelligent program algorithm is shown in Figure 3.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is an iteration counter and is equal to the number of the initial 1ms pulses applied to a particular 27C256 or 87C256 location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and Vpp = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

PROGRAM INHIBIT

Programming of multiple 27C256 or 87C256 EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or ALE/$\overline{CE}$ input inhibits other 27C256 or 87C256 EPROMs from being programmed.

Except for $\overline{OE}$, $\overline{CE}$, or ALE/$\overline{CE}$ all inputs of the parallel 27C256s or 87C256s may be common. A TTL low-level pulse applied to the $\overline{CE}$ or ALE/$\overline{CE}$ input with Vpp at 12.5V will program the selected 27C256 or 87C256.

VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL} and $\overline{CE}$ or ALE/$\overline{CE}$ at V_{IH}, and V_{PP} at 12.5V. Data should be verified a minimum of t_{OEV} after the falling edge of $\overline{OE}$.

Intelligent Identifier Mode

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C256 or 87C256.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the 27C256 or 87C256. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during intelligent identifier mode.

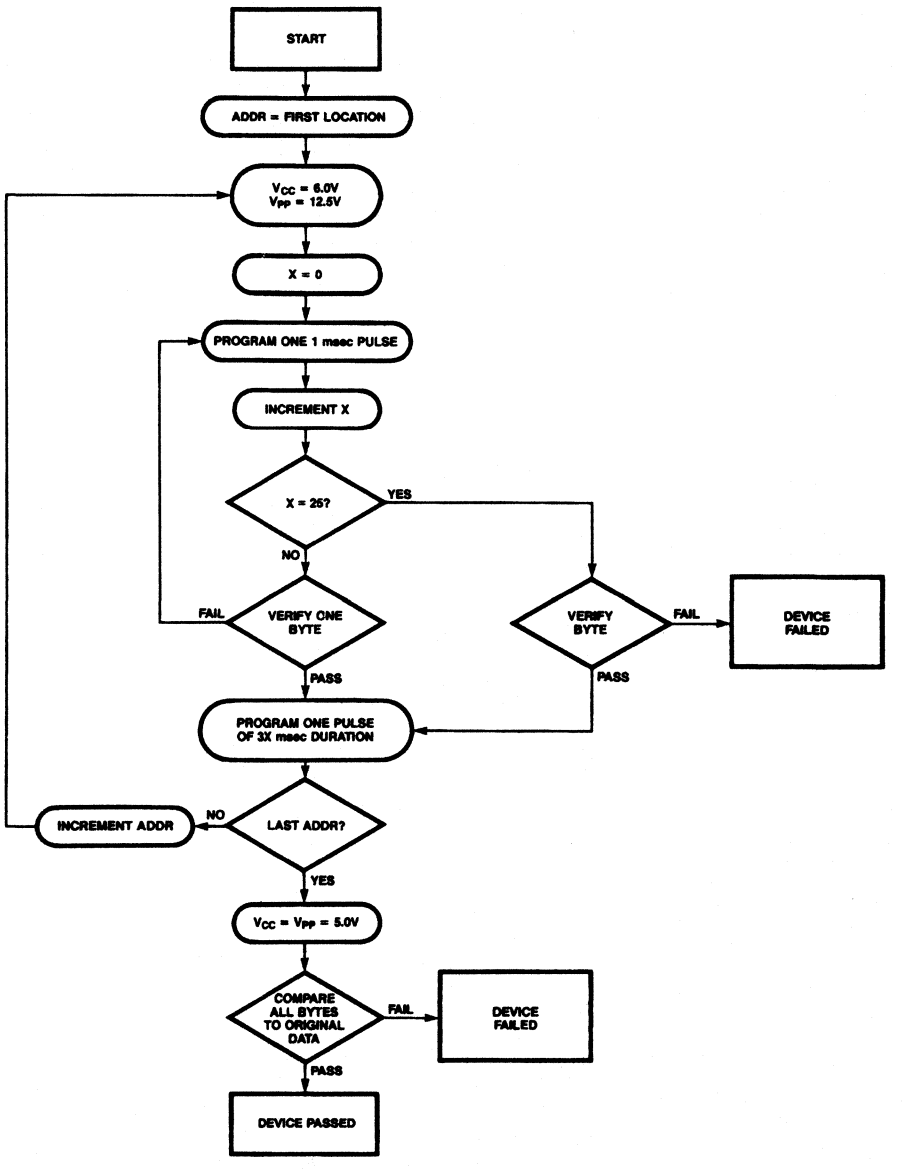


Figure 3. 27C256 and 87C256 Intelligent Programming Flowchart

INTELLIGENT PROGRAMMING ALGORITHM

DC PROGRAMMING CHARACTERISTICS: T_A = 25°C ±5°C, V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		
			Min	Max	Unit
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} + 0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	O_{0-7} = 0mA		30	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA

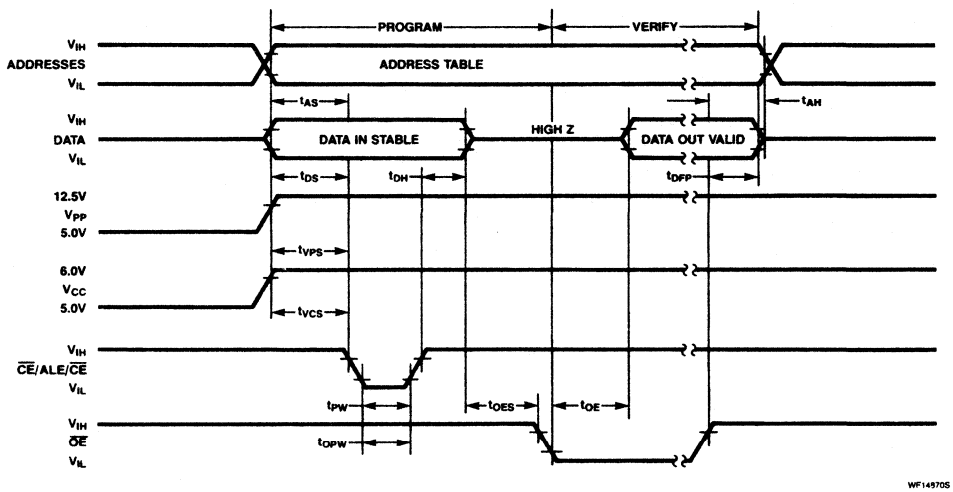
AC PROGRAMMING CHARACTERISTICS: 27C256/87C256

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			Min	Typ	Max	Unit
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[3]	$\overline{OE}$ high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{CE}$ initial program pulse width	(See Note 1)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width	(See Note 2)	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. Initial Program Pulse width tolerance is 1msec ±5%.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven - see timing diagram.



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C256/87C256, a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. When programming the 87C256, the address latch function is bypassed with V_{PP} at 12.5V. The device will function just like the 27C256 during read or write. When V_{PP} is at 5.0V during the read mode, the address latch function is enabled and $\overline{CE}$ needs to be toggled to latch in the addresses.

Figure 4. Intelligent Programming Waveforms: 27C256/87C256

Charge-Coupled Memory

317K-BIT CCD MEMORY

GENERAL DESCRIPTION

The SAA9001 is a 1-bit wide, 317,520 bits long charge-coupled shift register, organized in 294 blocks of 1080 bits each. It is intended for use in a tv field memory at a maximum frequency of 21,3 MHz.

The IC is encapsulated in a 28-pin dual-in-line package of which only fifteen pins are used. Power supplies of + 5 and −3,5 V are required. All inputs, outputs and controls are TTL-compatible.

Control is performed by two external signals, memory clock (MC) and memory gating (MG). The circuit has two data inputs (MI_1 and MI_2) and the data may be internally recirculated. An adjustable delay of 0 to 7 bits is incorporated at the output to increment the total delay on a bit-by-bit basis, as programmed by the inputs A0, A1 and A2.

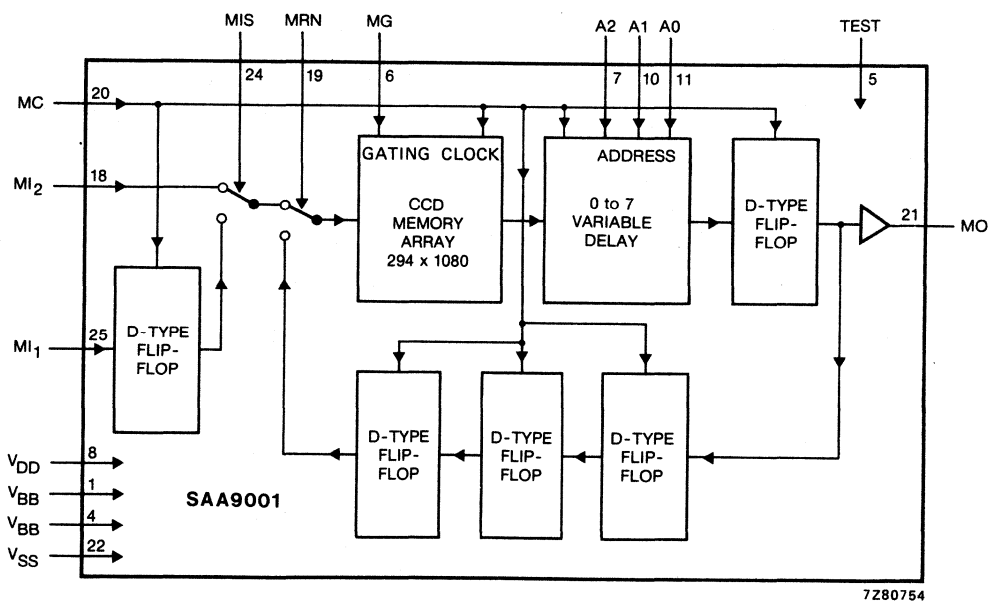


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA9001PB: 28-lead DIL; plastic (SOT-117).
SAA9001EB: 28-lead DIL; metal ceramic (cerdil) (SOT-87B).

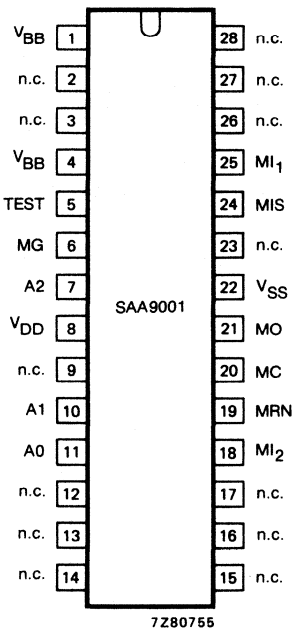


Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back-bias supply voltage (to be connected to pin 4)
4	V_{BB}	back-bias supply voltage (to be connected to pin 1)
5	TEST	control input for testing purposes only. It is internally connected to V_{SS} via a 1 kΩ (approx.) resistor and needs no external connection
6	MG	memory gating input
7	A2	control input for additional internal delay
8	V_{DD}	positive supply voltage
10	A1	control input for additional internal delay
11	A0	control input for additional internal delay
18	MI_2	memory input-2
19	MRN	memory recirculate control. Recirculation is activated when MRN is LOW
20	MC	memory clock input
21	MO	memory output
22	V_{SS}	negative supply voltage (ground)
24	MIS	memory input select; selects MI_1 or MI_2
25	MI_1	memory input-1

FUNCTIONAL DESCRIPTION

Operation

The memory array is organized to handle data in blocks of 1080 bits and has a capacity of 294 data blocks. The structure of the memory array provides fast, serial data input and output, with parallel transfer of data blocks through the memory. Memory input and output are controlled by the memory gating (MG), the serial output being initiated by the rising edge of MG and the storage of the data present in the memory's input register is performed on the falling edge of MG. In normal operation one cycle of MG is an uninterrupted HIGH level of at least 1080 clock periods (−4 or + 3 clock periods) followed by a LOW level of at least 32 clock periods. Input, output and gating signals are all referred to the rising edge of the memory clock (MC).

The internal recirculation facility is activated when the control input MRN is LOW.

Memory output

Output is enabled when MG is HIGH and data is clocked serially from the memory. Referring to Fig. 3, the first rising clock-edge after the positive transition of MG is defined as clock pulse "0". If the delay control address is A2 = A1 = A0 = 0, then the first bit of the output is valid at clock pulse "17" (the delay of 17 clock periods is due to internal multiplexing of the data in the memory).

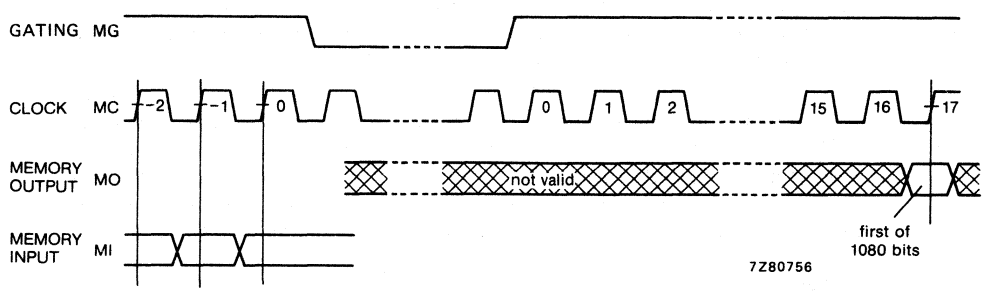


Fig. 3 Memory input and output data timings with respect to the memory clock (MC) for a memory gating (MG) HIGH period that is a multiple of 8 clock periods (no internal rounding of gating period).

The output delay can be increased by the values shown in Table 1 using the internal delay line controlled by A0, A1 and A2.

Table 1 Additional delay control

delay address			additional delay (clock periods)
A2	A1	A0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FUNCTIONAL DESCRIPTION (continued)

Data input

Data to be stored is directed to the memory from either MI_1 or MI_2 as selected by the control input MIS (see Table 2). The MI_1 input is delayed by one clock period.

Table 2 Input selection

control input	memory input
MIS = 0	MI_1
MIS = 1	MI_2

Input data is clocked serially into the input register of the CCD memory. When the negative transition of MG occurs, the 1080 bits of data present in the input register are entered into the memory array. If the interval of MG = HIGH is not an exact multiple of eight clock periods then the timing of the negative transition of MG is internally rounded to be an exact multiple of eight clock periods. Note that the data path from input MI_1 has a delay of one clock period and the path from MI_2 is direct.

The length of the MG = HIGH interval required for internal and external recirculation of data is determined as shown in Fig. 4. The positive transition of MG (waveform 1) initiates the serial transfer of data from the output register. Due to multiplexing in the memory, valid data is available after 16 clock periods (waveform 2). After a delay of "A" clock periods, determined by A0, A1 and A2 (waveform 3), and a one-clock-period delay via a D-type flip-flop, the valid data is available at the output pin MO (waveform 4).

Incoming data can be delayed by two amounts: RP (waveform 5), a phase shift introduced when the data is recirculated through an external processing circuit; and ID (waveform 6), a one-clock-period delay when input MI_1 is selected. The negative transition of MG, internally rounded to a multiple of eight clock periods (waveform 7), initiates storage of the last 1080 bits presented at the memory input (waveform 6). Therefore, the MG = HIGH interval is 16 + A + 1 + RP + ID + 1080 clock periods, and this figure is rounded to a multiple of eight. From this, (A + 1 + RP + ID) modulo 8 = 0.

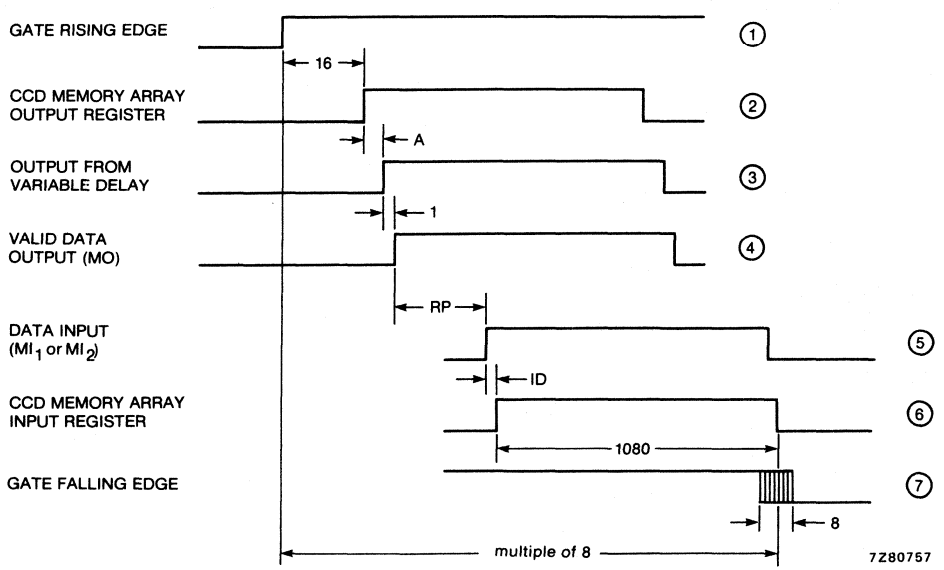


Fig. 4 Determination of memory gating HIGH period.

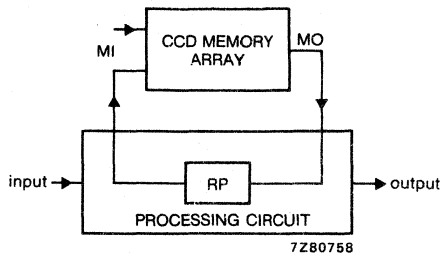


Fig. 5 Recirculation via an external circuit.

During internal recirculation of the data (MRN = LOW), the three D-type flip-flops in the recirculation path give RP a value of three clock periods and ID will be zero. Consequently, the variable delay should be programmed for a delay of A = 4 for proper data retention, i.e. (4 + 1 + 3 + 0) modulo 8 = 0.

In conclusion, to store 1080 bits of valid data and to retrieve at the output 1080 valid data bits, the MG = HIGH interval must be at least 1076 clock periods followed by an MG = LOW interval of at least 32 clock periods. The MG = LOW interval can be reduced to a minimum of 24 clock periods when MG = HIGH is a multiple of eight clock periods.

DEVELOPMENT DATA

Fast gating

Fast gating is a method of accelerating the internal transfer of data through the memory at the expense of valid data and is therefore useful for skipping unwanted data blocks. The MG = HIGH interval for fast gating is less than 1076 clock periods to a minimum of 360 clock periods. If the MG = HIGH interval is a multiple of eight clock periods during fast gating, the MG = LOW interval can be reduced to 24 clock periods (min.), otherwise the MG = LOW interval must be at least 32 clock periods. The output data is not valid during fast gating and during the first two data blocks at the output after fast gating has ceased. No valid data is clocked into the input register of the CCD memory during fast gating.

Slow gating

The transfer of data can be decelerated by using slow gating. For this, the MG = HIGH or MG = LOW interval is extended to the maximum waiting time (t_{GW}).

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Voltage on any pin, except V_{BB} (pin 4) and MO (pin 21), with respect to V_{SS}	V_I, V_O	max.	7 V
Back-bias voltage	V_{BB}	min.	−7 V
D.C. output current (sink or source)	I_O	max.	10 mA
Operating ambient temperature range (under d.c. operating conditions)	T_{amb}		0 to 60 °C
Storage temperature range	T_{stg}		−65 to 150 °C
Total power dissipation per package	P_{tot}		1 W

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CAPACITANCE

parameter	symbol	max.	unit
Capacitance at:			
data inputs MI_1, MI_2 (pins 25 and 18)	C_I	9	pF
clock input MC (pin 20)	C_C	9	pF
gating input MG (pin 6)	C_G	9	pF
data output MO (pin 21)	C_O	9	pF
recirculation control MRN (pin 19)	C_{RN}	9	pF
input select control MIS (pin 24)	C_{IS}	9	pF
delay program inputs A0, A1, A2 (pins 11, 10 and 7)	C_A	9	pF

D.C. OPERATING CONDITIONS

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	4,75	–	5,25	V
Back-bias supply range	V_{BB}	−3,65	–	−3,35	V
Input voltage LOW	V_{IL}	−1,0	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V

D.C. CHARACTERISTICS

T_{amb} = 0 to + 60 °C; V_{DD} = 4,75 to 5,25 V; V_{BB} = −3,5 ± 0,15 V; output not loaded; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input leakage current at V_i = GND to V_{DD}: MI_1; MI_2; MC; MG; A0; A1; A2; MRN; MIS	I_{LI}	–	–	10	μA
Power supply current from V_{DD} at f = 21,3 MHz	I_{DD}	–	–	70	mA
Output voltage LOW at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = −1 mA	V_{OH}	2,4	–	–	V

A.C. TEST CONDITIONS

Input pulse levels	0,6 and 2,4	V
Rise and fall times between 0,8 and 2,0 V (t_r, t_f)		
clock input MC	$\leqslant 3$	ns
data inputs MI_1, MI_2; gating input MG; control inputs A0, A1, A2, MIS, MRN	$\geqslant 3$	ns
Timing reference levels		
clock input MC	1,5	V
data inputs MI_1, MI_2 and gating input MG	0,8 or 2,0	V
data output MO	0,8 or 2,0	V
Output load	see Fig. 6	

A.C. CHARACTERISTICS

T_{amb} = 0 to 60 °C; V_{DD} = 4,75 to 5,25 V; V_{BB} = −3,5 ± 0,15 V

parameter	symbol	min.	typ.	max.	unit
Clock frequency (note 1)	f_{CL}	–	–	21,3	MHz
Clock LOW time	t_{CL}	18	–	–	ns
Clock HIGH time	t_{CH}	18	–	–	ns
Recirculation time (note 1)	t_R	–	–	27	ms
Waiting time (gating LOW/HIGH time) (note 2)	t_{GW}	–	–	1100	μs
Gating set-up time	t_{GC}	7,5	–	–	ns
Gating hold time	t_{CG}	0,5	–	–	ns
Data set-up time	t_{IC}	7,5	–	–	ns
Data hold time	t_{CI}	0,5	–	–	ns
Output hold time	t_{OH}	5,0	–	–	ns
Output delay time	t_{OD}	–	–	23,5	ns
Output invalid after address change	t_{AH}	0	–	–	μs
Address valid after address change (note 3)	t_{AD}	–	–	7 clock pulses + 1	μs
Recirculation set-up time (note 4)	t_{MRNSU}	0	–	1	μs
Input select set-up time (note 5)	t_{MISSU}	0	–	1 clock pulse + 1	μs

DEVELOPMENT DATA

Notes to the characteristics

1. The maximum recirculation time must never be exceeded by any combination of low frequency gating and/or waiting time.
2. Every 1300 μs at least three blocks of 1080 bits must be transferred to the output. This means that immediately after a wait of 1100 μs three blocks must be shifted out.
3. A change in delay will cause invalid data at the output for the time t_{AD}.
4. After a change of MRN, the signal recirculation path is not switched before t_{MRNSU}.
5. After a change of MIS, data at the input is invalid for t_{MISSU}.

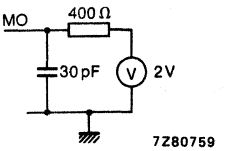


Fig. 6 Output load.

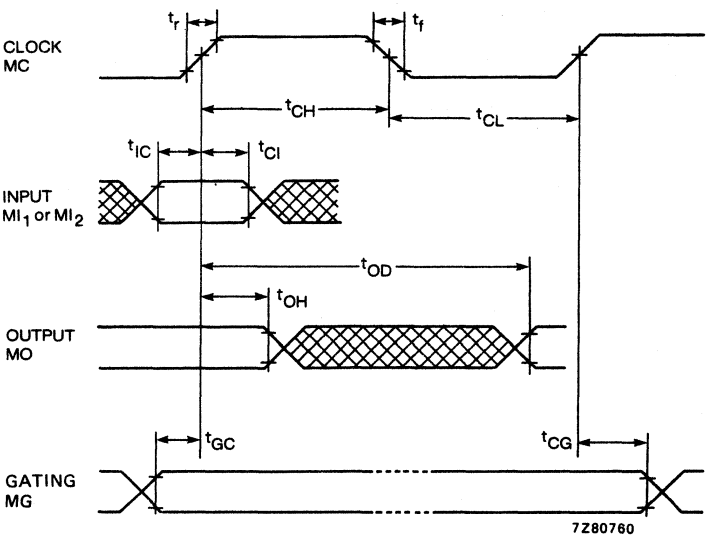


Fig. 7 Timing waveforms for gating and I/O.

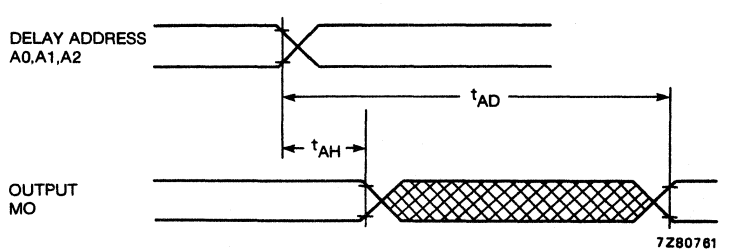


Fig. 8 Timing waveforms for address set-up and hold.

TTL MEMORIES

Introduction

Signetics

Quality and Reliability

Bipolar Memory Products

SIGNETICS' BIPOLAR MEMORY QUALITY

Signetics has put together a winning process for manufacturing Bipolar Memories. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The memories produced in both the Standard Products Division and the Application Specific Products Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from −55°C to +125°C and at +10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 — QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Bipolar Memory products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: T_J = 150°C, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): −65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam) and 300 cycles of thermal shock (−65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the bipolar memory SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors
- Device or generic group failure rate studies
- Advanced environmental stress development
- Failure mechanism characterization and corrective action/prevention reporting

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100ppm (parts per million), down from an industry practice of 10,000ppm, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

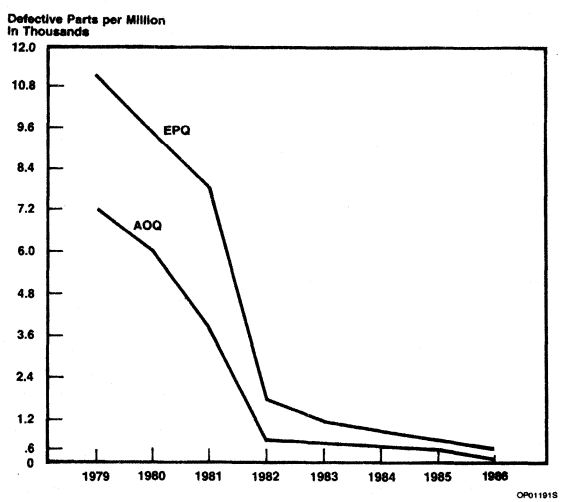


Figure 1. Signetics' Quality Progress

Quality and Reliability

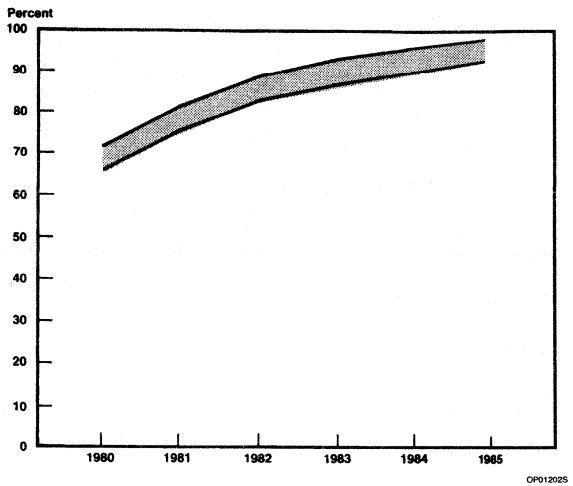


Figure 2. Performance To Schedule On-Time Delivery

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed-upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" — ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Quality and Reliability

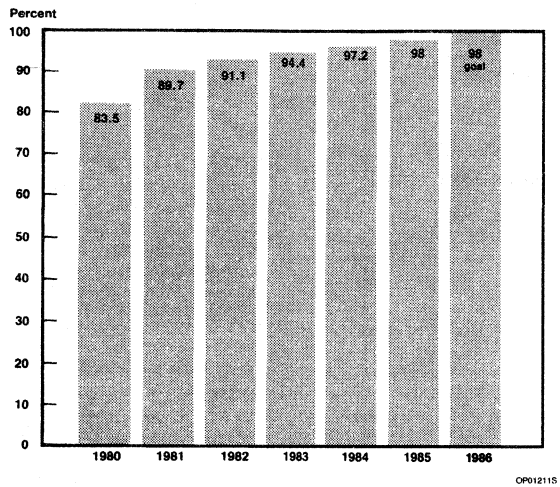


Figure 3. Lot Acceptance Rate From Signetics' Vendors

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1986 – 0
1985 – 0
1984 – 0
1983 – 0
1982 – 2
1981 – 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions:

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities — failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the corporate director of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Bipolar Memory Process Flow*, shows the result. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading quality supplier of bipolar memories. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

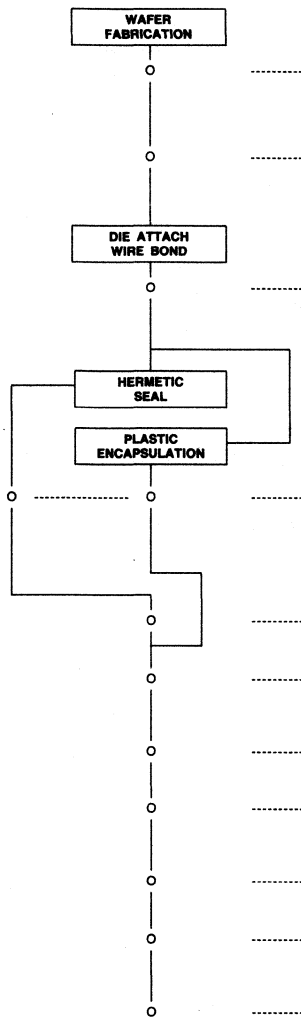
OUR GOAL: 100% PROGRAMMING YIELD

Our original goal back in the early 1970s was to develop a broad line of programmable products which would be recognized as having the best programming yield in the industry. Within the framework of a formal quality program, our efforts to improve circuit designs and refine manufacturing controls have resulted in major advances toward that goal.

Also within the framework of our formal quality program, we have now established a stated goal of 100% programming yield. Through the increasing effectiveness of a quality attitude of "Do It Right The First Time" we're moving ever closer to that target.

A significant amount of data on programming yields has been collected over the past two years. This data is the result of both inhouse programming (customer orders) and reports from major users of fuseable products. The data covers the full range of products from 256-bit PROMs to 64K PROMs and indicates an average level of 97.7% programming yield.

Quality and Reliability



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

STABILIZATION BAKE PRECONDITIONING

Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance. Hermetic devices are baked to ensure the elimination of any remaining cavity moisture.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% gross leak testing.

100% ELECTRICAL TEST

Every device is tested for functional and AC/DC parameters at 75°C with guard bands to assure performance to data sheet limits.

BURN IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum junction temperature.

SYMBOL

Devices are marked with the Signetics logo, device number and date code or custom symbol per individual specification requirements.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics or customer documents.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested for functional and AC/DC parameters at 25°C with guard bands to assure performance to data sheet limits.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step gurantees the specified mechanical and electrical AQL's. Every shipment is sealed and identified by QA personnel.

Figure 4. Bipolar Memory Process Flow

Quality and Reliability

As time goes on the drive for a product line that has Zero Defects will grow in intensity. These efforts will provide both Signetics and our customers with the ability to achieve the mutual goal of improved product quality.

The Bipolar Memory Quality Assurance department has monitored ppm progress, which can be seen in Figure 5. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

The real measure of any quality improvement program is the result that our customers see. The meaning of *Quality* is more than just working circuits. It means commitment to *On Time Delivery* at the *Right Place* of the *Right Quantity* of the *Right Product* at the *Agreed Upon Price.*

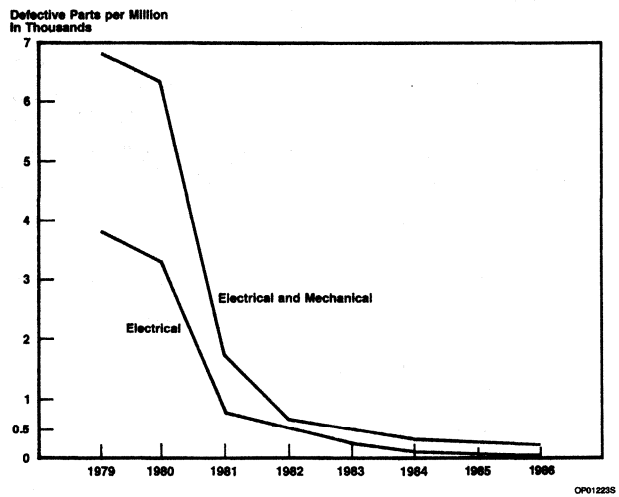


Figure 5. Bipolar Memory AOQ (Average Outgoing Quality)

Signetics

Selection Guide

Bipolar Memory Products

DEVICE[5]	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[3]	PACKAGE[4]	PINS	MAX I_{CC}
RAMs							
82S25	16 × 4	OC	B	50	N	16	105
3101A	16 × 4	OC	B	35	N	16	105
74S189	16 × 4	TS	B	35	N	16	110
74F189A	16 × 4	TS	—	20	N, A	16, 20	55
82S16	256 × 1	TS	T	50	N	16	115
74S301	256 × 1	OC	B	50	N	16	130
82LS16	256 × 1	TS	T	40	N	16	70
74LS301	256 × 1	OC	B	40	N	16	70
82S09	64 × 9	OC	T	45	A, N	28	190
82S09A	64 × 9	OC	T	35	A, N	28	190
82S19	64 × 9	OC	B	35	N	28	190
82S212	256 × 9	TS	B	45	N	22	185
82S212A	256 × 9	TS	B	35	N	22	185
8X350	256 × 8	TS	B	N/A	N	22	185
PROMs							
82S23	32 × 8	OC	—	50	N, A	16, 20	96
82S23A	32 × 8	OC	—	25	N, A	16, 20	96
82US23[6]	32 × 8	OC	—	10	N, A	16, 20	115
82S123	32 × 8	TS	—	50	N, A	16, 20	96
82S123A	32 × 8	TS	—	25	N, A	16, 20	96
82US123[6]	32 × 8	TS	—	10	N, A	16, 20	115
82S126	256 × 4	OC	—	50	N, A	16, 20	120
82S126A	256 × 4	OC	—	30	N, A	16, 20	120
82S129	256 × 4	TS	—	50	N, A	16, 20	120
82S129A	256 × 4	TS	—	27	N, A	16, 20	120
10149	256 × 4	OE	—	20	F	16	150
10149A	256 × 4	OE	—	10	F	16	160
100149	256 × 4	OE	—	20	F	16	150
100149A	256 × 4	OE	—	10	F	16	160
82S130	512 × 4	OC	—	50	N, A	16, 20	140
82S130A	512 × 4	OC	—	33	N, A	16, 20	140
82S131	512 × 4	TS	—	50	N, A	16, 20	140
82S131A	512 × 4	TS	—	30	N, A	16, 20	140
82LS135	256 × 8	TS	—	100	A, N	20	100
82S135	256 × 8	TS	—	45	A, N	20	150
82S115	512 × 8	TS	—	60	N	24	175
82S137	1024 × 4	TS	—	60	N, A	18, 20	140
82S137A	1024 × 4	TS	—	45	N, A	18, 20	140
82S137B	1024 × 4	TS	—	35	N, A	18, 20	140
82S137C[6]	1024 × 4	TS	—	25	N, A	18, 20	140
82S147	512 × 8	TS	—	60	A, N	20	155
82S147A	512 × 8	TS	—	45	A, N	20	155
82S147B[6]	512 × 8	TS	—	25	N, A	20	155
82LS181	1024 × 8	TS	—	120	A, N	24	80
82S181	1024 × 8	TS	—	70	N	24	175
82S181A	1024 × 8	TS	—	55	N, A	24, 28	175
82S181C	1024 × 8	TS	—	35	N, N3, A	24, 28	175
82S183	1024 × 8	TS	—	60	N, A	24, 28	175
82S185	2048 × 4	TS	—	100	N	18	120

Selection Guide

DEVICE[5]	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[3]	PACKAGE[4]	PINS	MAX I_{CC}
PROMs							
82S185A	2048 × 4	TS	—	50	N	18	155
82S185C[6]	2048 × 4	TS	—	25	N, A	18, 20	155
82HS187	1024 × 8	TS	R	55	N, A	24, 28	175
82HS187A	1024 × 8	TS	R	45	N, A	24, 28	175
82HS189	1024 × 8	TS	R	55	N, A	24, 28	175
82HS189A	1024 × 8	TS	R	45	N, A	24, 28	175
82HS191	2048 × 8	TS	—	20	N, N3, A	24, 28	175
82S191	2048 × 8	TS	—	80	N, A	24, 28	175
82S191A	2048 × 8	TS	—	55	N, A	24, 28	175
82S191C	2048 × 8	TS	—	35	A, N, N3	24	175
82HS195	4096 × 4	TS	—	45	N	20	145
82HS195A	4096 × 4	TS	—	35	N	20	145
82HS195B	4096 × 4	TS	—	25	N	20	145
82HS197[6]	2048 × 8	TS	R	65	N	24	175
82HS199[6]	2048 × 8	TS	R	65	N	24	175
82HS321	4096 × 8	TS	—	45	N, A	24, 28	175
82HS321A	4096 × 8	TS	—	35	N, A	24, 28	175
82HS321B	4096 × 8	TS	—	30	N, A	24, 28	175
82HS641	8192 × 8	TS	—	55	N	24, 28	175
82HS641A	8192 × 8	TS	—	45	N	24, 28	175
82HS641B	8192 × 8	TS	—	35	N	24, 28	175
82HS1281[6]	16384 × 8	TS	—	45	N	24	185

NOTES:

1. Output circuit
   OE = Open Emitter
   OC = Open Collector
   TS = 3-State
2. Output logic
   T = Transparent — input data appears on output during Write
   B = Blanked — output is blanked during Write
   R = Registers
   I/O = Programmable input/output option
3. Commercial (0°C to +75°C)
4. Packages:
   N = Plastic Dual In Line (N3 = 300mil-wide)
   A = Plastic Square Leaded Chip Carrier
   D = Small Outline Large (SO-L)
   *Whenever a single device is offered in both 300mil-wide and 600mil-wide packages, designate either N3 (300mil) or N (600mil) to assure proper order entry and shipment.
5. Part numbers:
   82Sxxx Junction-Isolated
   82HSxxx Oxide-Isolated
   82USxxx Oxide-Isolated TiW fuse
6. Objective specification (under product development)

Signetics

RAM Cross Reference Guide

Bipolar Memory Products

ORGANIZATION	PKG PINS	SIGNETICS	$\frac{T_{AA}}{I_{CC}}$	FAIRCHILD	$\frac{T_{AA}}{I_{CC}}$	TI	$\frac{T_{AA}}{I_{CC}}$	AMD	$\frac{T_{AA}}{I_{CC}}$	NATIONAL	$\frac{T_{AA}}{I_{CC}}$
16 × 4 OC	16	N3101A	$\frac{35}{105}$	93403*	NA	SN74S289B	$\frac{35}{105}$	AM27S02	$\frac{35}{100}$	DM74S289	$\frac{35}{110}$
								AM3101A	$\frac{35}{100}$		
16 × 4 TS	16	N74S189	$\frac{35}{110}$	93405*	NA	SN74S189B	$\frac{35}{110}$	AM27S03	$\frac{35}{100}$	DM74S189	$\frac{35}{110}$
		N74F189A	$\frac{15}{55}$					AM27S03A	$\frac{25}{100}$	DM74S189A	$\frac{25}{100}$
16 × 4 OC	16	N82S25	$\frac{50}{105}$	93403*	NA	SN74S289B	$\frac{35}{105}$	AM27S02	$\frac{35}{100}$	DM74S289	$\frac{35}{110}$
64 × 9 OC	28	N82S09	$\frac{45}{190}$								
		N82S09A T	$\frac{35}{190}$								
64 × 9 OC	28	N82S19	$\frac{35}{190}$	93419	$\frac{45}{150}$						
				93419A	$\frac{35}{150}$						
256 × 1 OC	16	N74S301	$\frac{50}{130}$			SN74S301	$\frac{65}{140}$	AM27LS01A	$\frac{35}{115}$		
256 × 1 OC	16	N74LS301	$\frac{40}{70}$					AM27LS01	$\frac{45}{70}$		
256 × 1 TS	16	N82S16 T	$\frac{50}{115}$	93421* T	NA	SN74S201	$\frac{65}{140}$	AM27LS00-1A T	$\frac{35}{115}$	74S200* T	NA
256 × 1 TS	16	N82LS16 T	$\frac{40}{70}$					AM27LS00-1 T	$\frac{45}{70}$	74S206* T	NA
256 × 8 TS	22	N8X350	$\frac{NA}{185}$								
256 × 9 TS	22	N82S212	$\frac{45}{185}$	93479	$\frac{45}{185}$						
		N82S212A	$\frac{35}{185}$	93479A	$\frac{35}{185}$						

NOTES:
T: Output is Transparent during write
*: Possibly Discontinued

Signetics

PROM Cross Reference Guide

Bipolar Memory Products

ORGANIZATION	PKG. PINS	SIGNETICS	MMI	TI	HARRIS*
32 × 8 OC	16	N82S23 N82S23A N82US23	63S080 63S080A	18SA030J, N	HM7602-5
32 × 8 TS	16	N82S123 N82S123A N82US123	63S081 63S081A	18S030J, N	HM7603-5
256 × 4 OC	16	N82S126 N82S126A	6300-1 63S140	24SA10J, N	HM7610-5 HM7610A-5 HM7610B-5
256 × 4 TS	16	N82S129 N82S129A	63S141	24S10J, N	HM7611-5 HM7611A-5 HM7611B-5
256 × 4 OE	16	10149** 10149A			
256 × 4 OE	16	100149** 100149A			
256 × 8 TS	20	N82S135			
256 × 8 TS	20	N82LS135		28L22J, N	
512 × 4 OC	16	N82S130 N82S130A	63S240		HM7620-5 HM7620A-5 HM7620B-5
512 × 4 TS	16	N82S131 N82S131A	63S241		HM7621-5 HM7621A-5 HM7621B-5
512 × 8 TS	20	N82S147 N82S147A N82S147B		28S42J, N	HM7649-5 HM7649A-5
512 × 8 TS	24	N82S141		28S46J, N	HM7641-5
512 × 8 TS	24	N82S115			HM7647R
1024 × 4 TS	18	N82S137 N82S137A N82S137B N82S137C	63S441 63S441A	24S41J, N	HM7643-5 HM7643A-5 HM7643B-5
1024 × 8 TS	24	N82S181 N82S181A N82S181C	63S881	28S86J, N 28S86-60J, N	HM7681-5 HM7681A-5
1024 × 8 TS	24	N82S181CN3			
1024 × 8 TS	24	N82LS181		28L86J, N	
1024 × 8 TS	24	N82S183			

* Discontinued Products
** ECL
***Planned New Product

PROM Cross Reference Guide

RAYTHEON	AMD	NATIONAL	FAIRCHILD	MOTOROLA	INTEL
	AM27S18AC AM27S185A	DM74S188			
	AM27S19AC AM27S195A	DM74S288			
29660C*	AM27S20C AM27S20AC	DM74S387 DM74S387A	93417C*		3601*
29661C*	AM27S21C AM27S21AC	DM74S287 DM74S287A	93427C*		3621*
			F10416** 10Z416**	MCM10149** 10149A**	
			F100416** 100Z416**		
		DM74LS471			
29610C*	AM27S12C AM27S12AC	DM74S570 DM74S570A	93436C*	MCM7620C	3602* 3602A*
29611C	AM27S13C AM27S13AC	DM74S571A DM74S571B	93446C*	MCM7621C	3622* 3622A*
29621C 29621AC	AM27S29C AM27S29A	DM74S472 DM74S472A			
29625C*	AM27S31C	DM74S474	93448C*	MCM7641C	3624* 3624A*
	AM27S15				
29641C*	AM27S33C AM27S33AC	DM74S573 DM74S573A DM74S573B	93453C	MCM7643C	3625*
29631C 29631AC	AM27S181C	DM87S181 DM87S181A	93Z451C	MCM7681C	3628*
	AM27S281A	DM87S281A			
			93L451C*		

PROM Cross Reference Guide

ORGANIZATION	PKG. PINS	SIGNETICS	MMI	TI	HARRIS*
1024 × 8 TS	24	N82HS187*** N82HS187A***	63RS881		
1024 × 8 TS	24	N82HS189*** N82HS189A***	63RS881		
2048 × 4 TS	18	N82S185 N82S185A N82S185C	– 63S841 63S841A	– 24S81J, N 24S81-55J, N	HM7685-5 HM7685A-5
2048 × 8 TS	24	N82HS191 N82S191 N82S191A N82S191C	63S1681A 63S1681	28S166J, N 38S165-35N	HM76161-5 HM76161A-5
2048 × 8 TS	24	N82S191CN3 N82HS197*** N82HS199***	63S168INS	38R165-20	
4096 × 4 TS	20 20	N82HS195 N82HS195A N82HS195B	63S1641 63S1641A		HM76165-5
4096 × 8 TS	24	N82HS321 N82HS321A N82HS321B	63S3281 63S3281A		
8192 × 8 TS	24	N82HS641 N82HS641A N82HS641B			HM76641-5 HM76641A-5
16384 × 8 TS	28	N82HS1281***			

* Discontinued Products
** ECL
***Planned New Product

PROM Cross Reference Guide

RAYTHEON	AMD	NATIONAL	FAIRCHILD	MOTOROLA	INTEL
	AM27S35C AM27S35AC				
	AM27S37C AM27S37AC	DM87SR181			
29651C 29651AC	AM27S185C AM27S185A	DM87S185 DM87S185A	93515C*	MCM7685C	
29681C 29681AC	AM27S191SA AM27S191C AM27S191AC	DM87S191 DM87S191A	93Z511C	MCM76161AC	3636B*
	AM27S291C AM27S291M AM27S47 AM27S45	DM87S291 DM77S291			
	AM27S41C AM27S41AC	DM87S195A DM87S195B	93513C*		
29671AC	AM27S43C AM27S43AC	DM87S321			
	AM27S49C AM27S49AC		93Z565C 93Z565AC		
	AM27S51				

Ordering Information

Bipolar Memory Products

Signetics Bipolar Memory intergrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

The table shown provides part number definition for Signetics memory products. The Signetics part number system allows complete definition for ordering a device. The part number itself and the product description is defined on each data sheet. The suffix is a single letter defining a package type (as shown in the table on this page). Additional or special processing is defined by adding the processing indicator when required.

The military qualification, Full MIL Signetics or Full JAN slash sheet status, can be determined by contacting Signetics Military Division or referring to the Signetics Military Data Book.

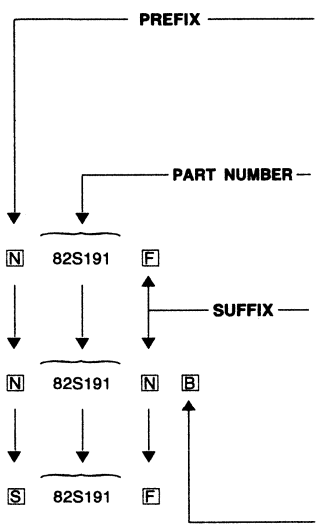


Table 1. Part Number Description

USED TO DEFINE OPERATING TEMPERATURE RANGE	
Prefix	**Device Temperature Range**
N	0°C to +75°C
S	−55°C to +125°C

USED TO DEFINE PART ITSELF

USED TO DEFINE PACKAGE TYPE	
Package Code	**Package Description**
A	28-Leaded Plastic Chip Carrier
D	16, 20-Lead Small Outline
F	16, 18, 20, 22, 24, 28-Lead CERDIP
N	16, 18, 20, 22, 24, 28-Lead DIP Plastic
N3	24-Lead 300mil-wide DIP Plastic

PROCESSING INDICATOR

COMMERCIAL		
B	SUPR II B	Operating High Temp. Burn-In

64-bit TTL Bipolar RAM

Signetics

82S25
3101A
74S189
64-Bit TTL Bipolar RAM

Bipolar Memory Products

Product Specification

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature PNP inputs and 1 Chip Enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

Ordering information can be found on the following page.

The 82S25 and 74S189 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

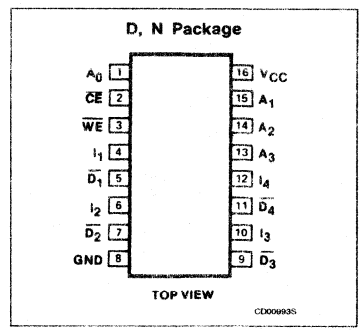
FEATURES

- **Output access time:**
  - **N82S25: 50ns max**
  - **N3101A: 35ns max**
  - **N74S189: 35ns max**
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S25: Open Collector**
  - **N3101A: Open Collector**
  - **N74S189: 3-State**
- **Schottky clamped**
- **TTL compatible**

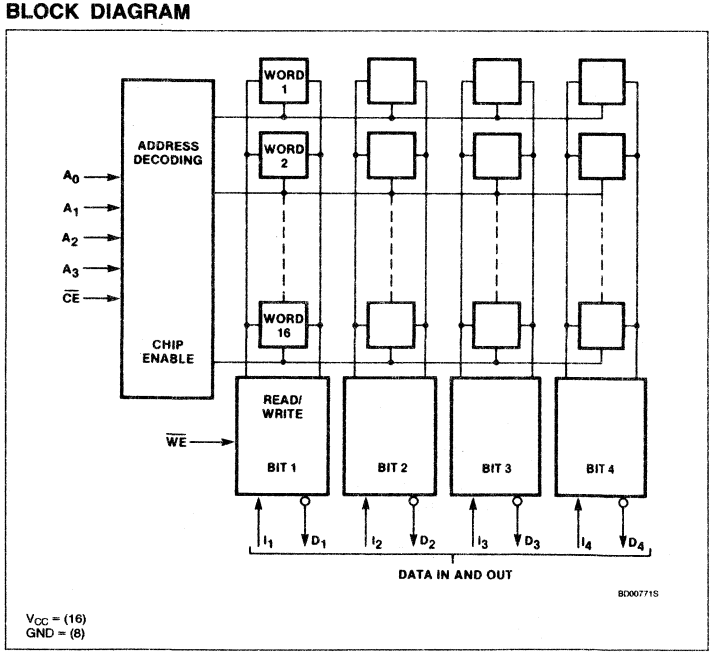
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S25 N • N3101A N • N74S189 N
16-pin Plastic Small Outline 300mil-wide	N82S25 D • N3101A D • N74S189 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[1]						
V_{IL} V_{IH} V_{IC}	Low High Clamp[7]	V_{CC} = 4.75V V_{CC} = 5.25V I_{IN} = −12mA, V_{CC} = 4.75V	2.0		0.8 −1.5	V
Output voltage[1]						
V_{OL} V_{OH}	Low[2,3] High (74S189)	$\overline{CE}$ = Low I_{OUT} = 16mA, V_{CC} = 4.75V I_{OUT} = −2mA	2.4		0.45	V
Input current[5]						
I_{IL} I_{IH}	Low High	V_{IN} = 0.45V V_{IN} = 5.5V			−100 10	μA
Output current[5]						
I_{OLK} I_{OS} I_{OZ}	Leakage Short circuit (74S189) Hi-Z (74S189)	$\overline{CE}$ = High, V_{OUT} = 5.5V, V_{CC} = 4.75V $\overline{CE}$ = Low, V_{OUT} = 0V $2.4 \geq V_{OUT} \geq 0.4V$			100 −100 ±50	μA mA μA
Supply current[6]						
I_{CC}	82S25 3101A 74S189	V_{CC} = 5.25V V_{CC} = 5.25V V_{CC} = 5.25V			105 105 110	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	V_{CC} = 5.0V V_{IN} = 2.0V V_{OUT} = 2.0V, $\overline{CE}$ = High		5 8		pF

TRUTH TABLE

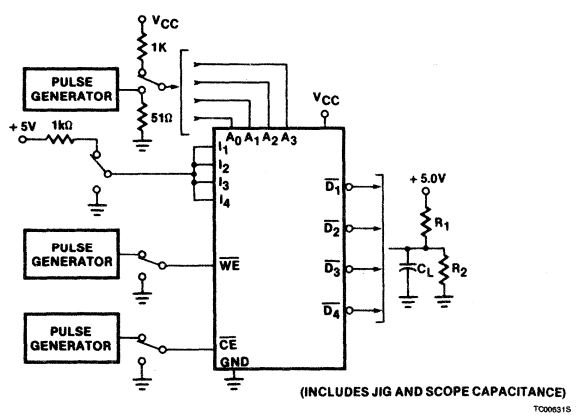
MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	74S189
				Data Out		
Read	0	1	X	Stored $\overline{Data}$	Stored $\overline{Data}$	Stored $\overline{Data}$
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S25			N3101A, N74S189			UNIT
				Min	Typ	Max	Min	Typ	Max	
Access time										
t_{AA} t_{CE}	Address Chip enable					50 35			35 17	ns
Disable time[8]										
t_{CD}		Output	Chip enable			35			17	ns
Response time[8]										
t_{WD}		Output	Write enable			25			25	ns
Write recovery time										
t_{WR}						50			35	ns
Setup and hold time										
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write enable	Address	5 5			0 0			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	30 5			25 0			
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	0 5			0 0			
Pulse width[4]										
t_{WP}[10]	Write enable			30			25			ns

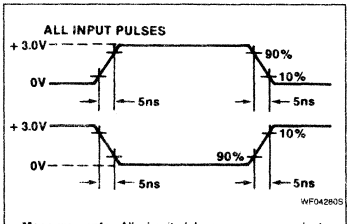
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the outputs open.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Conditions

VOLTAGE WAVEFORM

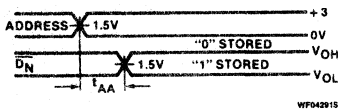


Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

Input Pulses

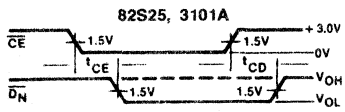
TIMING DIAGRAMS

Read Cycle



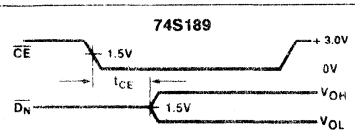
Address Access Time

82S25, 3101A

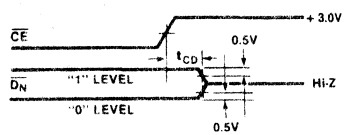


Chip Enable/Disable Times

74S189

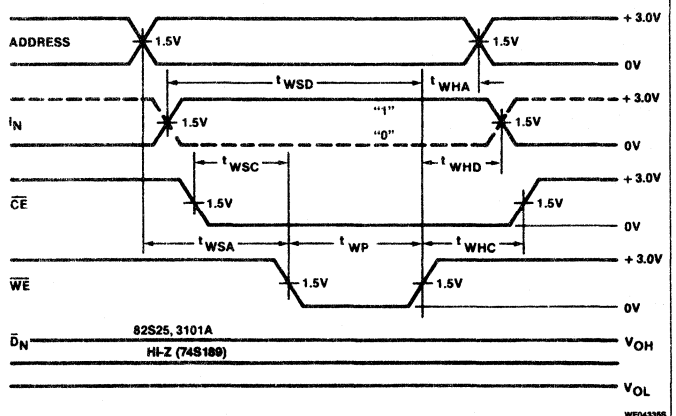


Chip Enable



Chip Disable

Write Cycle



Signetics

74F189A
64-Bit TTL Bipolar RAM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 74F189A is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the high-impedance state whenever the Chip Select ($\overline{CE}$) input is High. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Ordering information can be found on the following page.

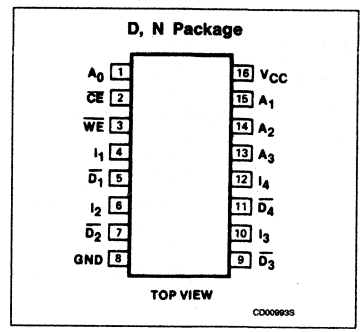
FEATURES

- **Address access time: 15ns max**
- **Power dissipation: 4.3mW/bit typ**
- **Schottky clamped TTL**
- **One Chip Enable input**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

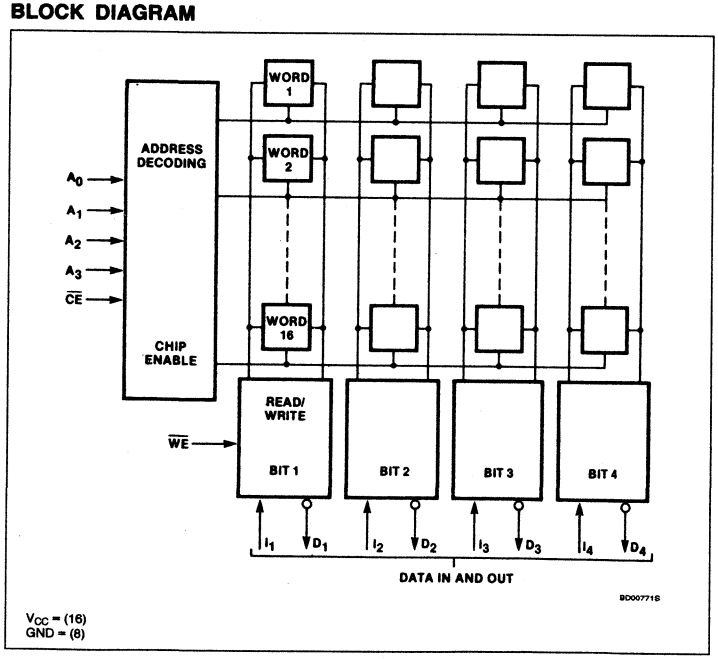
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION



BLOCK DIAGRAM



64-Bit TTL Bipolar RAM (16 × 4) — 74F189A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N74F189A N
16-pin Plastic Small Outline 300mil-wide	N74F189A D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V_{DC}
V_{IN}	Input voltage	−0.5 to +7.0	V_{DC}
V_{OH}	Output voltage High	−0.5 to +5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IC}[7]	Clamp	V_{CC} = 5.25V, I_I = −18mA			−1.2	V
Output voltage						
V_{OH} V_{OL}[2,3]	High Low	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V I_{OH} = −3.0mA I_{OL} = 20mA	2.4	 0.35	 0.5	V
Input current						
I_{IH} I_{IL}	High Low	V_{CC} = 5.25V V_{IN} = 5.5V V_{IN} = 0.5V			40 0.6	µA
Output current						
I_{OZ} I_{OS}	Off-state Short circuit	V_{CC} = 5.25V V_{IH} = 2.0V, 2.4V ≥ V_{OUT} ≥ 0.5V V_{CC} = 5.25V	 −60		±50 −150	µA mA
Supply current[6]						
I_{CC}		V_{CC} = 5.25V, $\overline{WE}$, $\overline{CE}$ = GND			70	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	V_{CC} = 5.0V V_{IN} = 2.0V V_{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	DATA OUT
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

X = Don't care

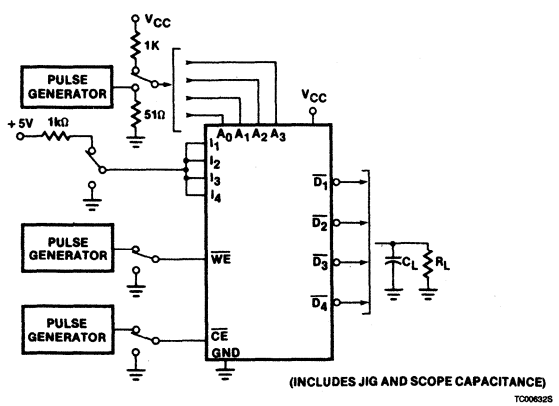
64-Bit TTL Bipolar RAM (16 × 4) — 74F189A

AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Access time							
t_{AA} t_{CE}	Address Chip enable					15 13	ns
Disable time[8]							
t_{CD}		Output	Chip enable			9	ns
Response time[8]							
t_{WD}		Output	Write enable			9	ns
Write recovery time							
t_{WR}		Output	Write enable			13	ns
Setup and hold time							
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write enable	Address	3 2			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	13 2			
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	3 2			
Pulse width[4]							
t_{WP}[10]	Write enable			10			ns

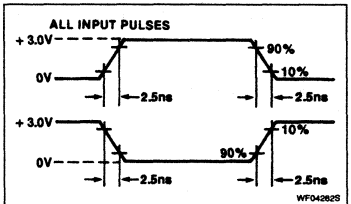
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Conditions

VOLTAGE WAVEFORM

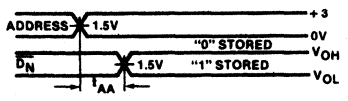


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and output.

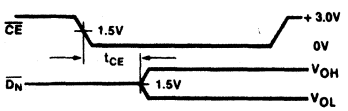
Input Pulses

TIMING DIAGRAMS

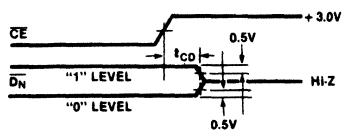
Read Cycle



Address Access Time

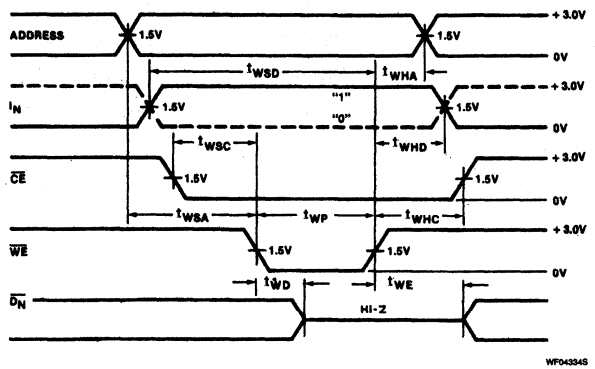


Chip Enable



Chip Disable

Write Cycle



All AC parameters are measured at 1.5V unless otherwise specified.

256-bit TTL Bipolar RAM

Signetics

82S16
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82S16 has fast Read access and Write cycle times, and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

The 82S16 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data book.

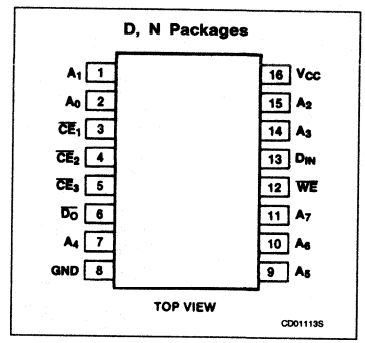
FEATURES

- **Address access time: 50ns max**
- **Write cycle time: 50ns max**
- **Power dissipation: 1.5mW/bit typ**
- **Input loading: −100μA max**
- **Output follows complement of data input during Write**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **Output: 3-State**
- **Schottky clamped**
- **TTL compatible**

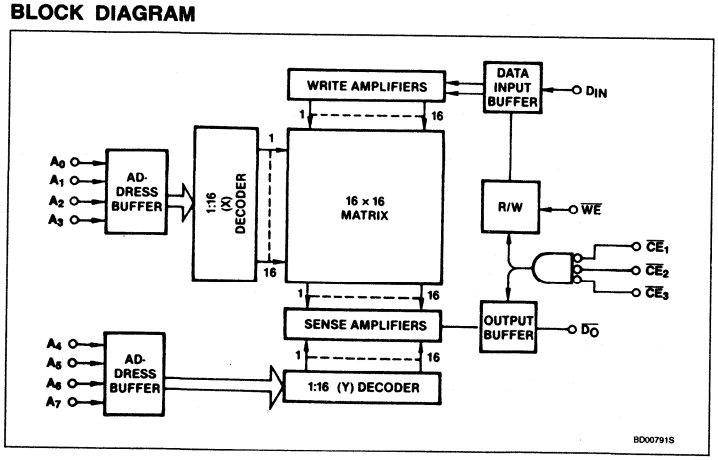
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1) — 82S16

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S16 N
16-pin Plastic Small Outline 300mil-wide	N82S16 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open collector)	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IL}	Low	V_{CC} = Min			0.8	
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−1.0	−1.5	
Output voltage[2]						
V_{OH}	High	V_{CC} = Min I_{OH} = −3.2mA	2.6			V
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45	
Input current[3]						
I_{IH}	High	V_{CC} = Max V_{IN} = 5.5V		1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	
Output current						
I_{OZ}	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[7]	V_{CC} = Max, V_O = 0V	−15		−70	mA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		80	115	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

*"0" = All $\overline{CE}$ inputs Low; "1" = One or more $\overline{CE}$ inputs High. X = Don't care.

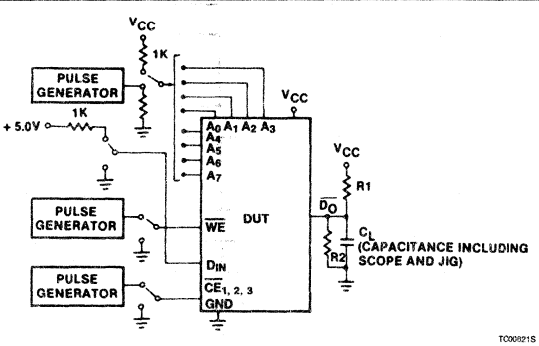
256-Bit TTL Bipolar RAM (256 × 1) — 82S16

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA}	Address	Output	Address		40	50	ns
t_{CE}	Chip enable	Output	Chip enable		30	40	
Disable time[10]							
t_{CD}		Output	Chip enable		30	40	ns
t_{WD}	Valid time	Output	Write enable		30	40	
Setup and hold time							
t_{WSA}[11]	Setup time	Write enable	Address	15	5		ns
t_{WHA}	Hold time			5	0		
t_{WSD}	Setup time	Write enable	Data in	40	30		
t_{WHD}	Hold time			5	0		
t_{WSC}	Setup time	Write enable	$\overline{CE}$	10	0		
t_{WHC}	Hold time			5	0		
Pulse width[9]							
t_{WP}[12]	Write enable			30	15		ns

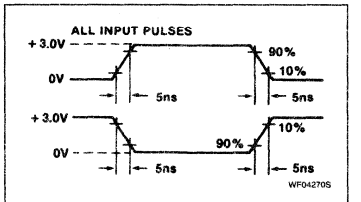
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

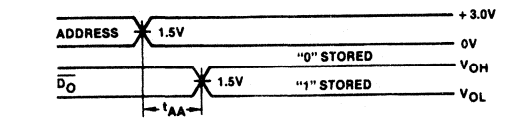
VOLTAGE WAVEFORM



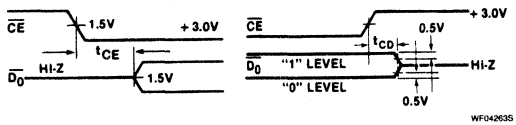
Measurements:
All circuit delays are measured at the+1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAMS

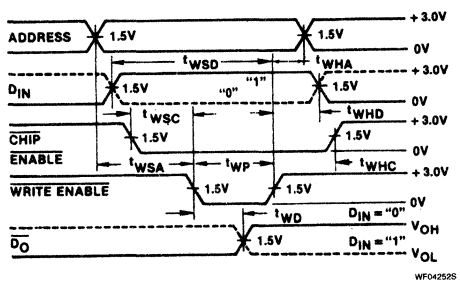


Address Access Time



Chip Enable | Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

Signetics

82LS16
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82LS16 has fast Read access and Write cycle times, as well as low power requirements and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Ordering information can be found on the following page.

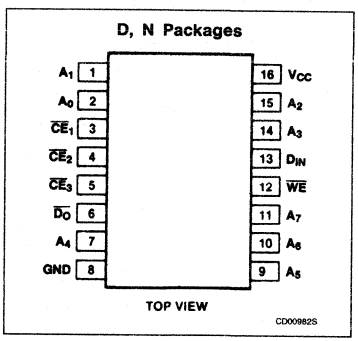
FEATURES

- **Address access time: 40ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.98mW/bit typ**
- **Input loading: −100μA max**
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Three Chip Enable inputs**
- **Output: 3-State**
- **Schottky clamped**
- **TTL compatible**

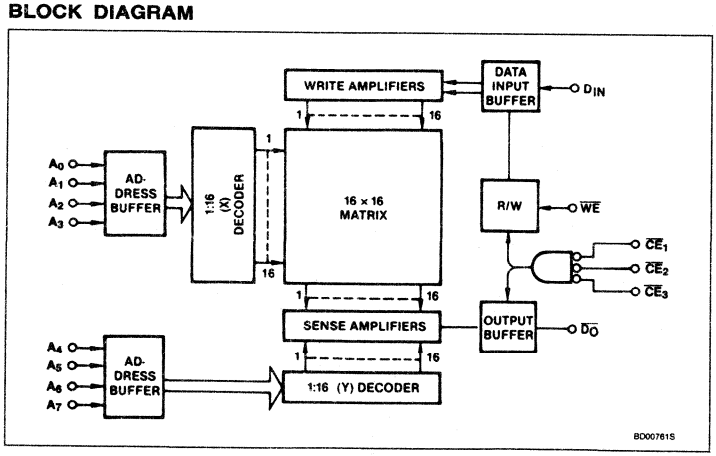
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1) — 82LS16

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82LS16 N
16-pin Plastic Small Outline 300mil-wide	N82LS16 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open collector)	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IL}	Low	V_{CC} = 4.75V			0.8	
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA		−1.0	−1.5	
Output voltage[2]						
V_{OH}	High	V_{CC} = 4.75V I_{OH} = −3.2mA	2.6			V
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45	
Input current[3]						
I_{IH}	High	V_{CC} = 5.25V V_{IN} = 5.5V		1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	
Output current						
I_{OZ}	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[7]	V_{CC} = 5.25V, V_O = 0V	−15		−70	mA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		50	70	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

*"0" = All $\overline{CE}$ inputs Low; "1" = One or more $\overline{CE}$ inputs High. X = Don't care.

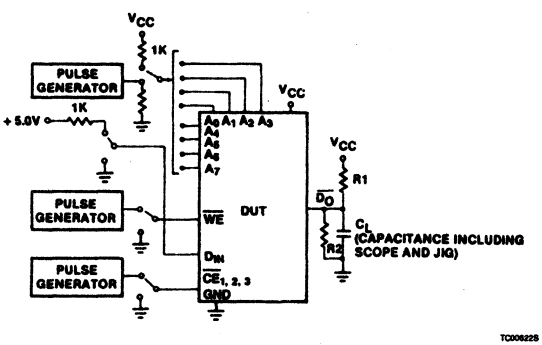
256-Bit TTL Bipolar RAM (256 × 1) — 82LS16

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA}	Address	Output	Address		30	40	ns
t_{CE}	Chip enable	Output	Chip enable		15	25	
Disable time[10]							
t_{CD}		Output	Chip enable		15	25	ns
t_{WD}	Valid time	Output	Write enable		30	40	
Setup and hold time							
t_{WSA}[11]	Setup time	Write enable	Address	0	−5		ns
t_{WHA}	Hold time			0	−5		
t_{WSD}	Setup time	Write enable	Data in	25	15		
t_{WHD}	Hold time			0	−5		
t_{WSC}	Setup time	Write enable	$\overline{CE}$	0	−5		
t_{WHC}	Hold time			0	−5		
Pulse width[9]							
t_{WP}[12]	Write enable			25	15		ns

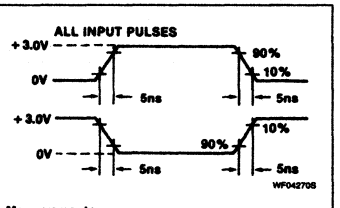
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

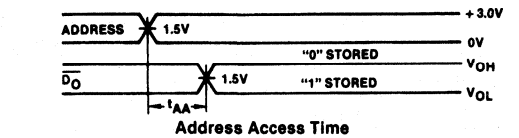
VOLTAGE WAVEFORM



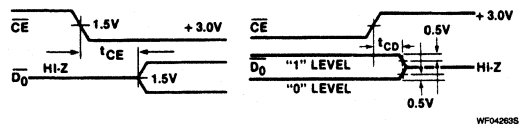
Measurements:
All circuit delays are measured at the+1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAMS

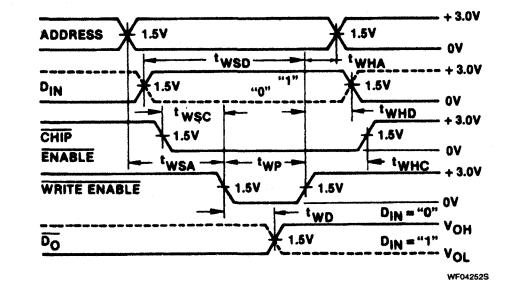


Address Access Time



Chip Enable | Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

Signetics

74S301
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 74S301 is a Read/Write memory array which features an Open Collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write ($\overline{D_O}$ terminal High) permits $\overline{D_O}$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

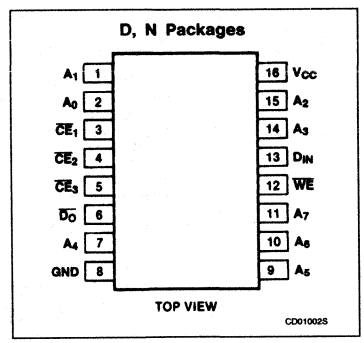
FEATURES

- **Address access time: 50ns max**
- **Write cycle time: 55ns max**
- **Power dissipation: 1.5mW/bit typ**
- **Input loading: −100μA max**
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**
- **Three Chip Enable inputs**
- **Output: Open Collector**

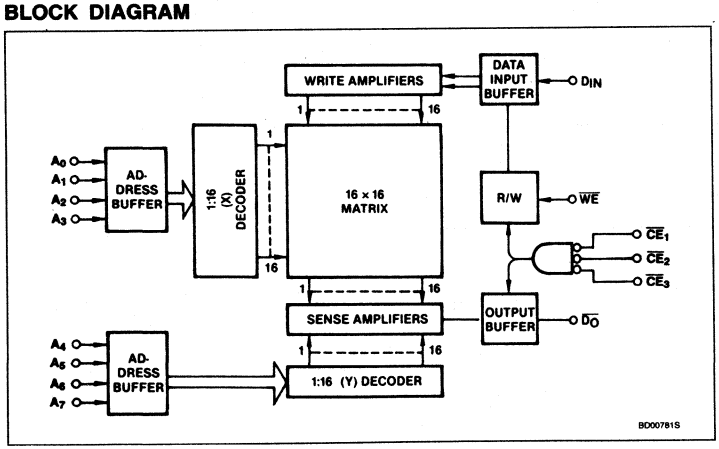
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1) — 74S301

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N74S301 N
16-pin Plastic Small Outline 300mil-wide	N74S301 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open collector)	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage						
V_{IL} V_{IH} V_{IC}	Low High Clamp[3]	V_{CC} = 4.75V V_{CC} = 5.25V V_{CC} = 4.75V, I_{IN} = −12mA	2.0	 −1.0	0.8 −1.2	V
Output voltage						
V_{OL}	Low[5]	V_{CC} = 4.75V I_{OL} = 16mA		0.35	0.45	V
Input current						
I_{IL} I_{IH}	Low High	V_{CC} = 5.25V V_{IL} = 0.45V V_{IH} = 2.7V			−100 25	μA
Output current						
I_{OLK}	Leakage	V_{IH} = 2V, V_O = 5.5V			40	μA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V, T_A = +125°C		80	130	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	V_{CC} = 5.0V V_{IN} = 2.0V V_{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

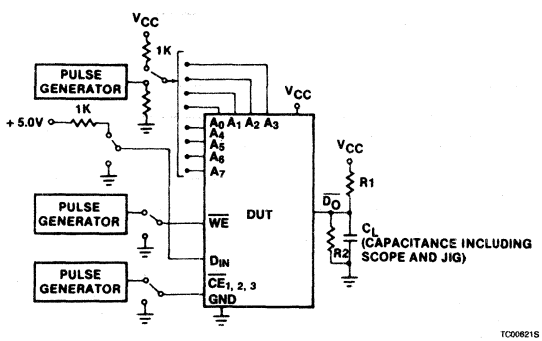
*"0" = All $\overline{CE}$ inputs Low: "1" = One or more $\overline{CE}$ inputs High.
X = Don't care.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA} t_{CE}	Address Chip enable	Output Output	Address Chip enable		40 30	50 40	ns
Disable time[10]							
t_{CD} t_{WD}	Valid time	Output Output	Chip enable Write enable		30 30	40 40	ns
Setup and hold time							
t_{WSA}[11] t_{WHA}	Setup time Hold time	Write enable	Address	20 5	5 0		ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	40 5	30 0		
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	10 5	0 0		
Pulse width[9]							
t_{WP}[12]	Write enable			30	15		ns

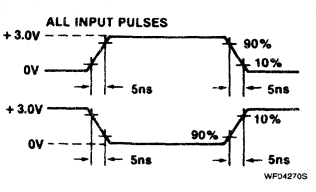
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

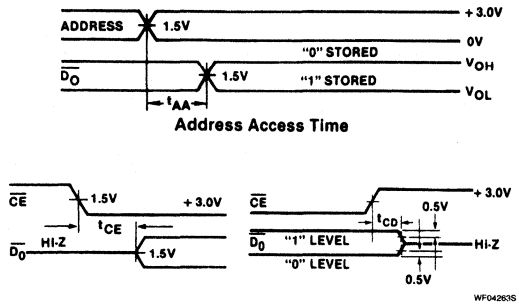
VOLTAGE WAVEFORM

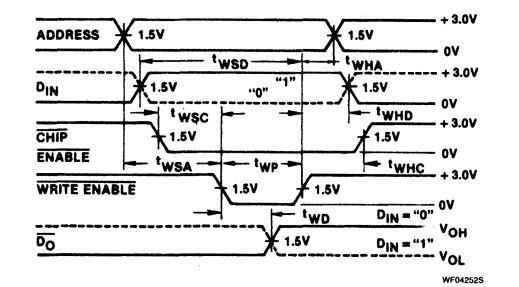


MEASUREMENTS:
All circuit delays are measured at the+1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAMS





NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

Signetics

74LS301
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 74LS301 is a Read/Write memory array which features an Open Collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write ($\overline{D_O}$ terminal High) permits $\overline{D_O}$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

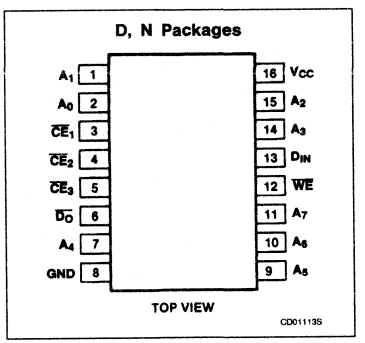
FEATURES

- **Address access time: 40ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.98mW/bit typ**
- **Input loading: −100μA max**
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**
- **Three Chip Enable inputs**
- **Open Collector output**

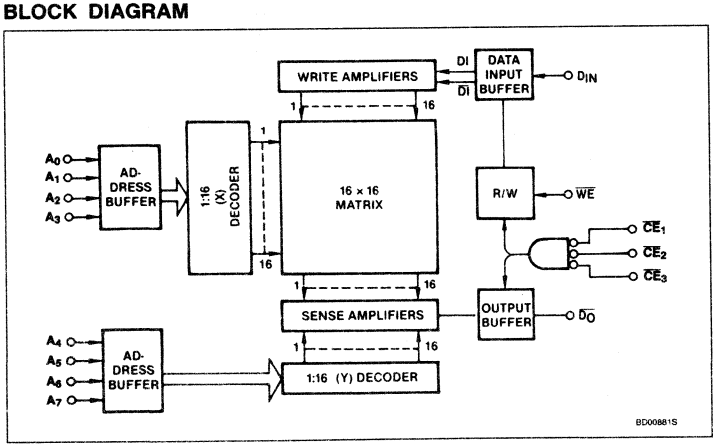
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1) — 74LS301

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N74LS301 N
16-pin Plastic Small Outline 300mil-wide	N74LS301 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open collector)	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA			−1.2	
Output voltage						
V_{OL}	Low[5]	V_{CC} = 4.75V I_{OL} = 16mA			0.45	V
Input current[2]						
I_{IL}	Low	V_{CC} = 5.25V V_{IL} = 0.45V			−100	μA
I_{IH}	High	V_{IH} = 2.7V			25	
Output current						
I_{OLK}	Leakage[5]	V_{IH} = 2V, V_O = 5.5V			40	μA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		50	70	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

*"0" = All $\overline{CE}$ inputs Low: "1" = One or more $\overline{CE}$ inputs High.
X = Don't care.

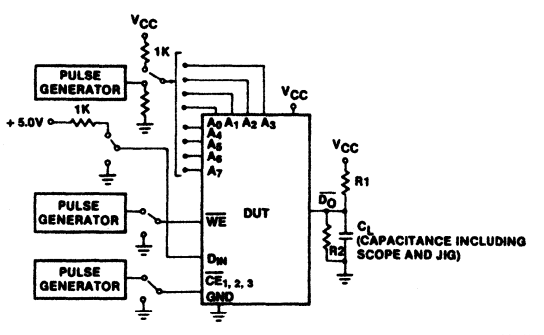
256-Bit TTL Bipolar RAM (256 × 1) — 74LS301

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA}	Address	Output	Address		30	40	ns
t_{CE}	Chip enable	Output	Chip enable		15	25	
Disable time[10]							
t_{CD}		Output	Chip enable		15	25	ns
t_{WD}	Valid time	Output	Write enable		30	40	
Setup and hold time							
t_{WSA}[11]	Setup time	Write enable	Address	0	−5		ns
t_{WHA}	Hold time			0	−5		
t_{WSD}	Setup time	Write enable	Data in	25	15		
t_{WHD}	Hold time			0	−5		
t_{WSC}	Setup time	Write enable	$\overline{CE}$	0	−5		
t_{WHC}	Hold time			0	−5		
Pulse width[9]							
t_{WP}[12]	Write enable			25	15		ns

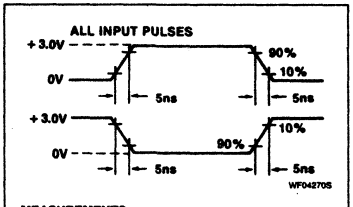
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from logic levels with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

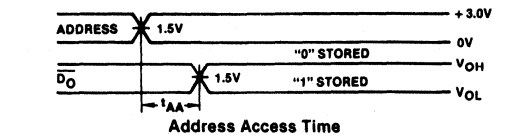
VOLTAGE WAVEFORM



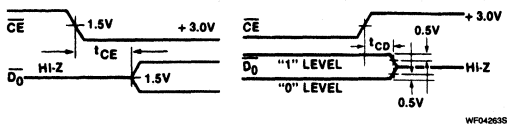
MEASUREMENTS:
All circuit delays are measured at the+1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAMS

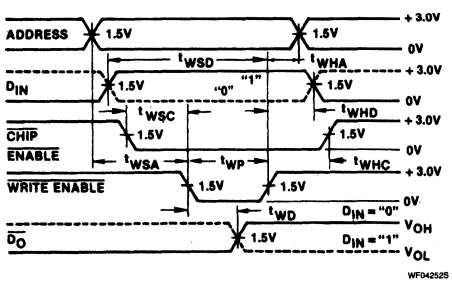


Address Access Time



Chip Enable | Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

Byte-Organized RAM

Signetics

82S09
82S09A
576-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/09A features Open Collector outputs, Chip Enable input, and a very low current PNP input structure to enhance memory expansion.

Ordering information can be found on the following page.

The 82S09 and 82S09A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

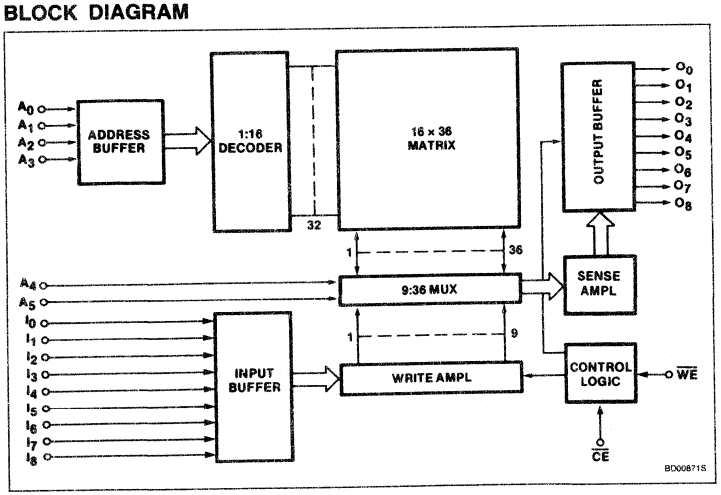
FEATURES

- **Address access time:**
  - **N82S09: 45ns max**
  - **N82S09A: 35ns max**
- **Write cycle time:**
  - **N82S09/09A: 45ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **Output is non-blanked during Write**
- **One Chip Enable input**
- **Outputs: Open Collector**

APPLICATIONS

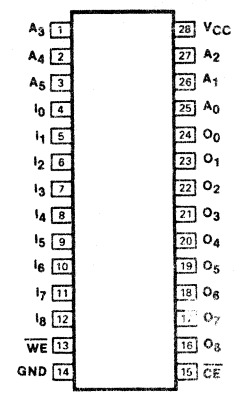
- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

BLOCK DIAGRAM



PIN CONFIGURATIONS

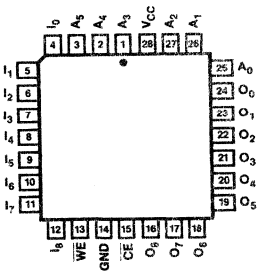
N Package



TOP VIEW

CD11036S

A Package



TOP VIEW

CD12590S

576-Bit TTL Bipolar RAM (64 × 9) — 82S09, 82S09A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	N82S09 N · N82S09A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S09 A · N82S09A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[1]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			
V_{IC}	Clamp[2]	V_{CC} = 4.75V Min, I_{IN} = −12mA			−1.5	
Output voltage[1]						
V_{OL}	Low[3]	V_{CC} = 4.75V, I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			25	
Output current						
I_{OLK}	Leakage[4]	V_{CC} = 5.25V, V_{OUT} = 5.5V			40	μA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V			190	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

Refer to notes on next page.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	O_N
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

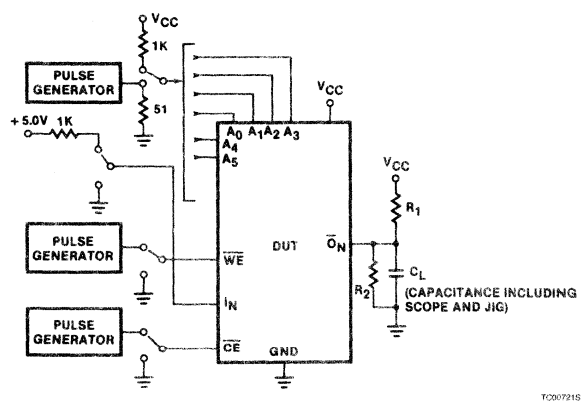
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S09			N82S09A			UNIT
				Min	Typ	Max	Min	Typ	Max	
Access time										
t_{AA}	Address					45			35	ns
t_{CE}	Chip enable					30			25	
Disable time[8]										
t_{CD}		Output	Chip enable			30			25	ns
t_{WA}	Valid time	Output	Write enable			30			25	
Setup and hold time										
t_{WSA}[9]	Setup time	Write	Address	5			5			ns
t_{WHA}	Hold time	enable		5			5			
t_{WSD}	Setup time	Write	Data in	35			30			
t_{WHD}	Hold time	enable		5			5			
t_{WSC}	Setup time	Write	$\overline{CE}$	5			5			
t_{WHC}	Hold time	enable		5			5			
Pulse width[6]										
t_{WP}[10]	Write enable			35			35			ns

NOTES:
1. All voltage values are with respect to network ground.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is applied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the Write enable and chip enable input grounded, all other inputs at 0.45V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
8. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

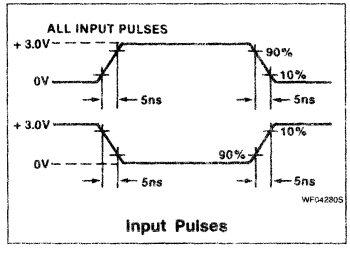
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

Loading Condition

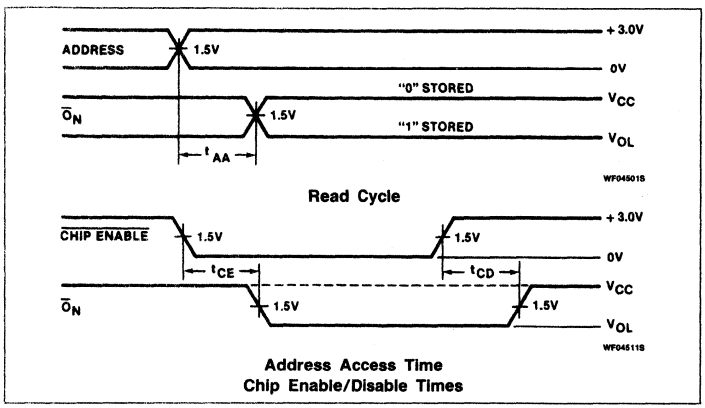
VOLTAGE WAVEFORM

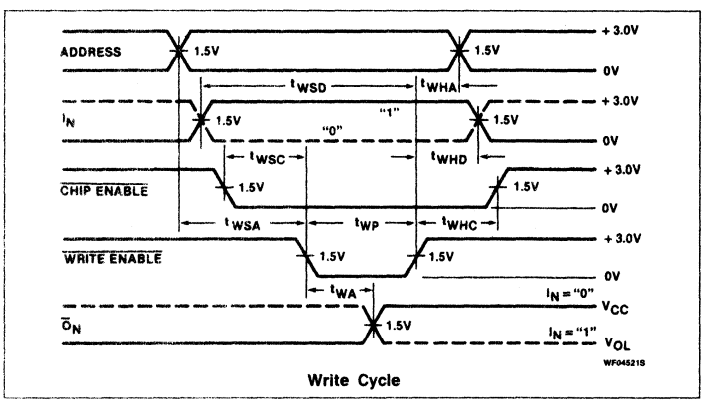


Input Pulses

576-Bit TTL Bipolar RAM (64 × 9) — 82S09, 82S09A

TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes High (blanks).
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid.)
t_{WA}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.

Signetics

82S19
576-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S19 features Open Collector outputs, Chip Enable input, and a very low current PNP input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

Ordering information can be found on the following page.

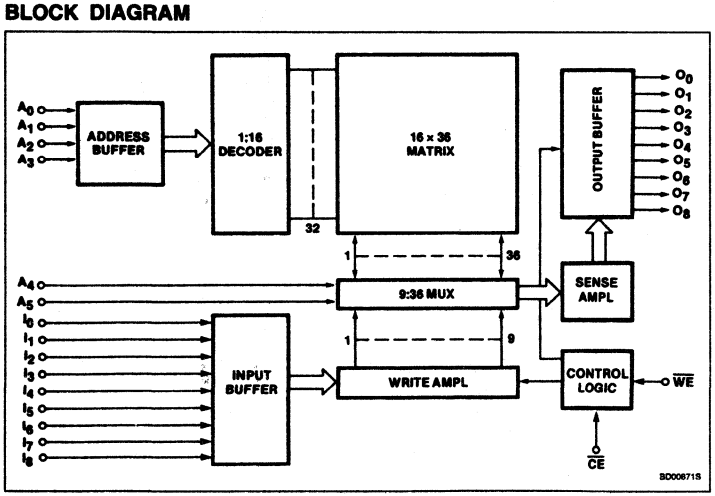
FEATURES

- **Address access time: 35ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Output is blanked during Write**
- **Outputs: Open Collector**

APPLICATIONS

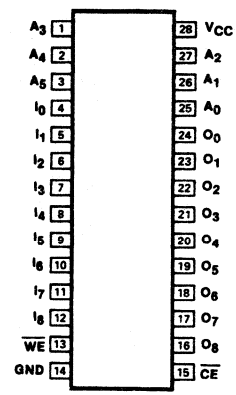
- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

BLOCK DIAGRAM

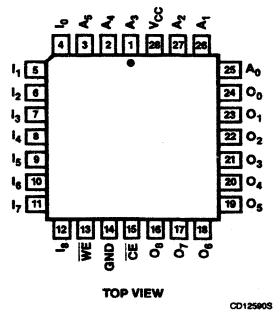


PIN CONFIGURATIONS

N Package



A Package



576-Bit TTL Bipolar RAM (64 × 9) — 82S19

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	N82S19 N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S19 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low	$V_{CC} = 4.75V$			0.8	V
V_{IH}	High	$V_{CC} = 5.25V$	2.0			
V_{IC}	Clamp[2]	$V_{CC} = 4.75V$, $I_{IN} = -12mA$			−1.5	
Output voltage						
V_{OL}	Low[3]	$V_{CC} = 4.75V$, $I_{OL} = 8.0mA$			0.5	V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			26	
Output current						
I_{OLK}	Leakage[4]	$V_{CC} = 5.25V$, $V_{OUT} = 5.5V$			40	μA
Supply current[3,5]						
I_{CC}		$V_{CC} = 5.25V$			190	mA
Capacitance						
		$V_{CC} = 5.0V$				pF
C_{IN}	Input	$V_{IN} = 2.0V$		5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

Refer to notes on next pages.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{O}_N$
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care

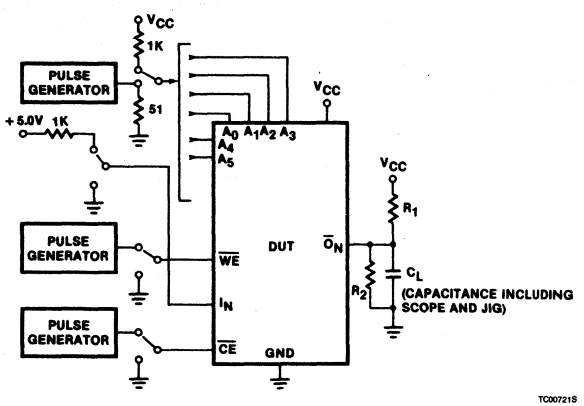
576-Bit TTL Bipolar RAM (64 × 9) — 82S19

AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Access time							
t_{AA}	Address					35	ns
t_{CE}	Chip enable					25	
t_{CD}	Disable time	Output	Chip enable			25	ns
t_{WD}	Valid time	Output	Write enable			25	
t_{WR}	Write recovery time	Output	Write enable			25	
Setup and hold time							
t_{WSA}[8]	Setup time	Write enable	Address	5			ns
t_{WHA}	Hold time			5			
t_{WSD}	Setup time	Write enable	Data in	30			
t_{WHD}	Hold time			5			
t_{WSC}	Setup time	Write enable	$\overline{CE}$	5			
t_{WHC}	Hold time			5			
Pulse width[6]							
t_{WP}[9]	Write enable			35			ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the Write enable and chip enable inputs grounded, all other inputs at 0.45V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
8. Measured with minimum t_{WP}.
9. Measured with minimum t_{WSA}.

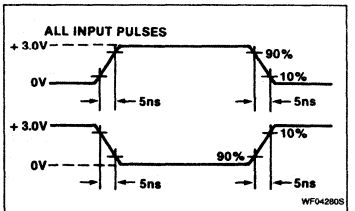
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

Loading Condition

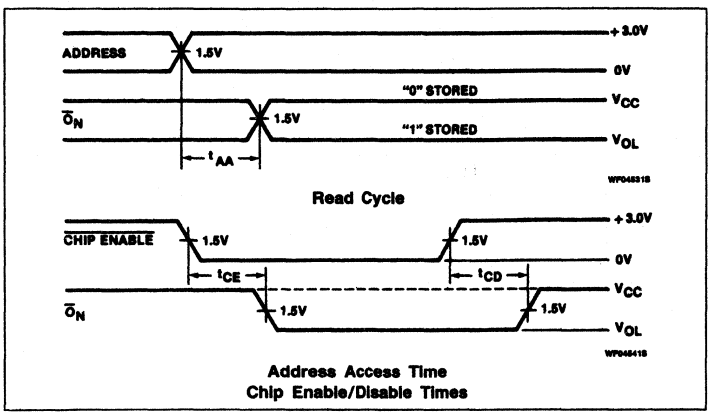
VOLTAGE WAVEFORM

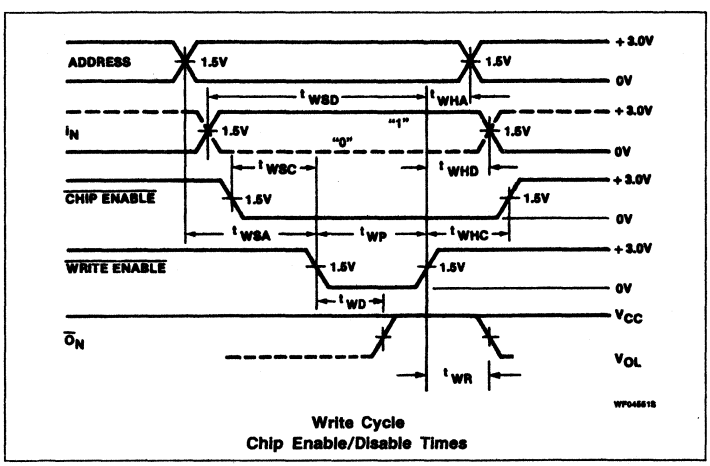


Input Pulses

576-Bit TTL Bipolar RAM (64 × 9) — 82S19

TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes High (blanks).
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid.)

Signetics

82S212
82S212A
2304-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of the 82S212 and 82S212A allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 and 82S212A are ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

Data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of Read/Write operations using a common bus.

Ordering information can be found on the following page.

The 82S212 and 82S212A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

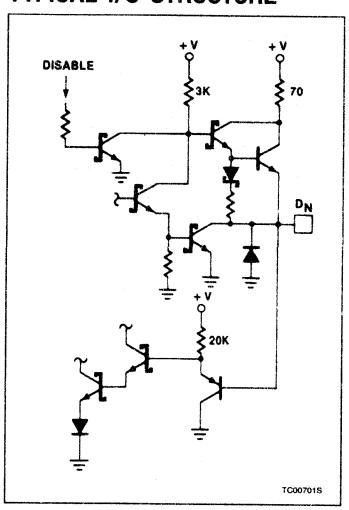
FEATURES

- **Address access time:**
  - **N82S212: 45ns max**
  - **N82S212A: 35ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Schottky clamped TTL**
- **One Chip Enable input**
- **Common I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

APPLICATIONS

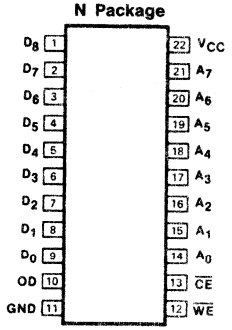
- **Cache memory**
- **Buffer storage**
- **Writable control store**

TYPICAL I/O STRUCTURE



PIN CONFIGURATIONS

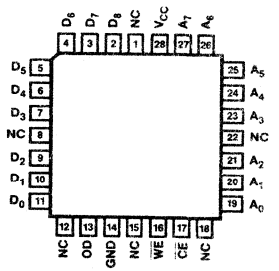
N Package



TOP VIEW

CD01002S

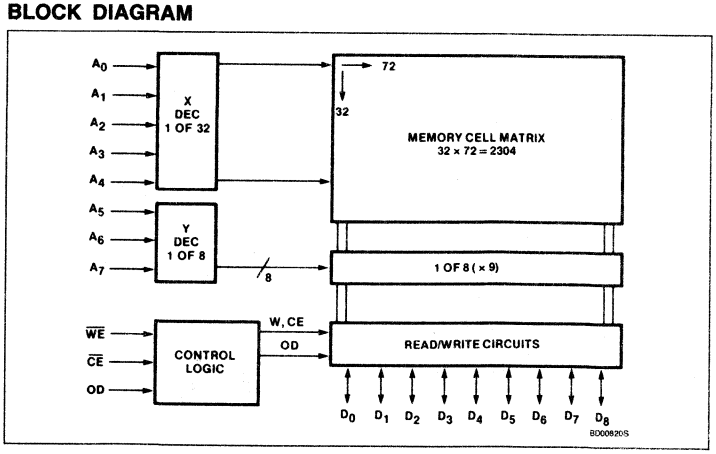
A Package



TOP VIEW

CD12600S

BLOCK DIAGRAM



2304-Bit TTL Bipolar RAM (256 × 9) — 82S212, 82S212A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Plastic DIP 400mil-wide	N82S212 N · N82S212A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S212 A · N82S212A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open collector)	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IL}	Low	$V_{CC} = 4.75V$			0.80	V
V_{IH}	High	$V_{CC} = 5.25V$	2.0			
V_{IC}	Clamp[4]	$V_{CC} = 4.75V$, $I_{IN} = -12mA$			−1.5	
Output voltage[2]						
V_{OH}	High	$I_{OH} = -2mA$	2.4			V
V_{OL}	Low	$V_{CC} = 4.75V$, $I_{OL} = 8.0mA$			0.5	
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			25	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, or OD = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High or OD = High, $V_{OUT} = 0.5V$			−100	
I_{OS}	Short circuit[4,5]	$\overline{CE}$ = OD = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		135	185	mA
Capacitance						
		$V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	Hi-Z
Disable R/W	X	1	X	Hi-Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

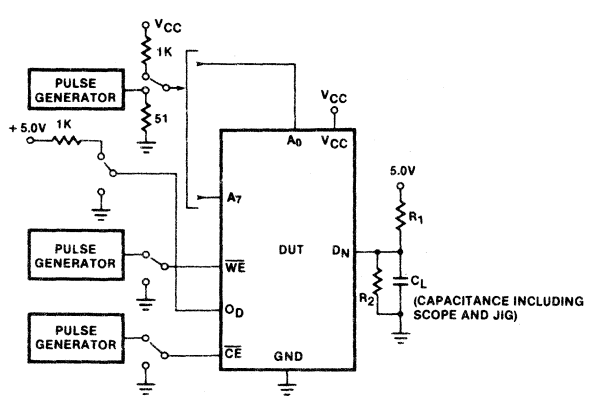
2304-Bit TTL Bipolar RAM (256 × 9) — 82S212, 82S212A

AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[1]	TO	FROM	N82S212			N82S212A			UNIT
				Min	Typ[3]	Max	Min	Typ[3]	Max	
Access time										
t_{AA}	Address	Output	Address			45			35	ns
Enable time										
t_{OE}	Output	Output	OD	5		25			25	ns
t_{CE}	Output	Output	Chip enable			25			25	
Disable time[6]										
t_{OD}	Output	Output	OD			25			25	ns
t_{CD}	Output	Output	Chip enable			25			25	
Pulse width										
t_{WP}[8]	Write			25			25			ns
Setup and hold time										
t_{SWC}	Setup time	Write	Chip enable	5			5			ns
t_{WHD}	Hold time	Chip enable	Write	5			5			
t_{WSD}	Setup time	Write	Data	25			25			
t_{WHD}	Hold time	Data	Write	5			5			
t_{WSA}[9]	Setup time	Write	Address	5			5			
t_{WHA}	Hold time	Address	Write	5			5			
t_{SO}	Setup time (from disabled state)	Chip enable	OD	5			5			
t_{HO}	Hold time	OD	Chip enable	5			5			

NOTES:
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the outputs open.
8. Measured with minimum t_{WSA}.
9. Measured with minimum t_{WP}.

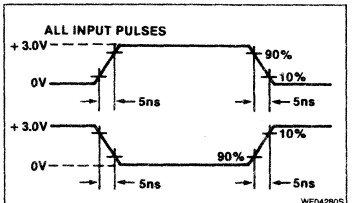
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

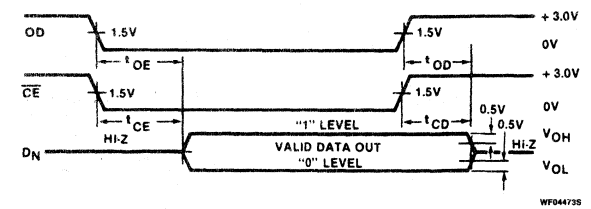
Loading Condition

VOLTAGE WAVEFORM



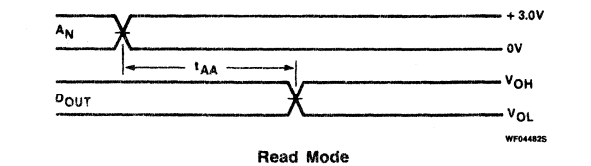
Input Pulses

TIMING DIAGRAMS

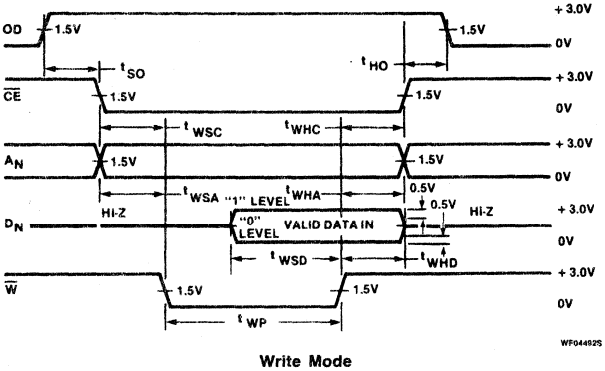


Enable/Disable

NOTE:
Assumes T_{AA} from address to valid data $\overline{W}$ = High



Read Mode



Write Mode

CAUTION:
Data Bus conflict can occur with $\overline{CE}$ = 0, apply data source after T_{OD}(max.) and remove data source before T_{OE}(min.).

Signetics

8X350
2K-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-State outputs.

Ordering information can be found on the following page.

The 8X350 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

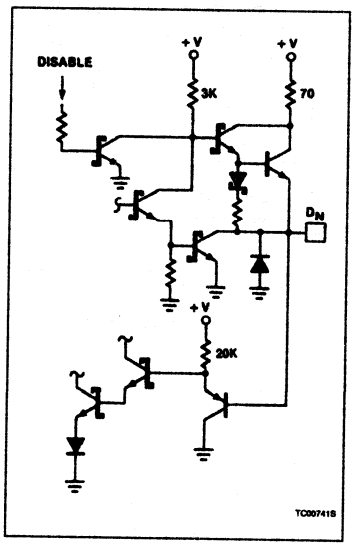
FEATURES

- **On-chip address latches**
- **Schottky clamped**
- **One Master Enable input**
- **Directly interfaces with the 8X305 bipolar microprocessor with no external logic**
- **May be used on left or right bank**
- **Common I/O:**
  - **Inputs: PNP buffered**
  - **Outputs: 3-State**

APPLICATIONS

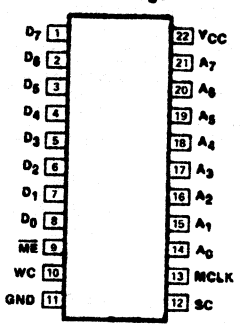
- **8X300 or 8X305 working storage**

TYPICAL I/O STRUCTURE

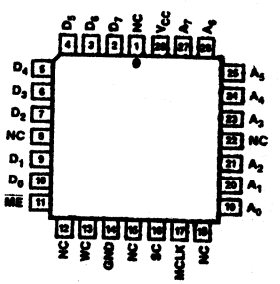


PIN CONFIGURATIONS

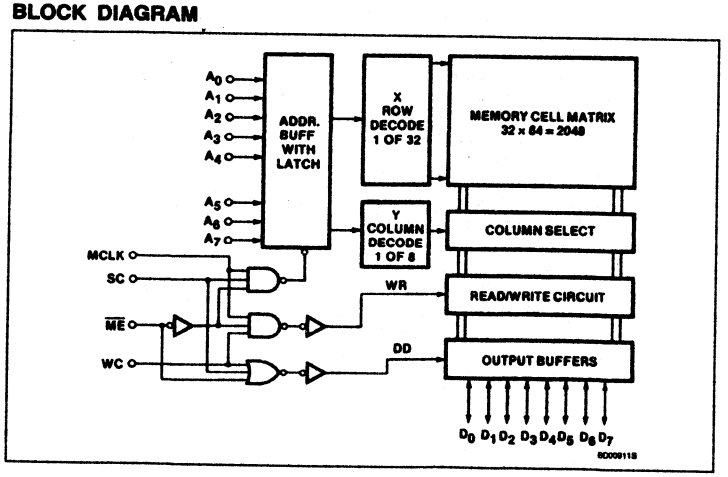
N Package



A Package



BLOCK DIAGRAM



2K-Bit TTL Bipolar RAM (256 × 8) — 8X350

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Plastic DIP 400mil-wide	N8X350 N
28-pin Plastic Leaded Chip Carrier 450mil-square	N8X350 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
	Output voltage		
V_{OH}	High	+5.5	V_{DC}
V_O	Off-stage	+5.5	
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA			−1.2	
Output voltage						
		V_{CC} = 4.75V				
V_{OL}	Low[4]	I_{OL} = 9.6mA			0.5	V
V_{OH}	High[5]	I_{OH} = −2mA	2.4			
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			25	
Output current						
I_{OZ}	Hi-Z State	$\overline{ME}$ = High, V_{OUT} = 5.5V			40	μA
		$\overline{ME}$ = High, V_{OUT} = 0.5V			−100	
I_{OS}	Short circuit[3,6]	SC = WC, $\overline{ME}$ = Low,				
		V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			185	mA
Capacitance						
		$\overline{ME}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

TRUTH TABLE

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address Disable data out	1	X	X	X	Hi-Z data out
Input new address	0	1	0	1	Address Hi-Z
Hold address Disable data out	0	1	0	0	Hi-Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	Hi-Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	–
Hold address[12] Disable data out	0	1	1	0	Hi-Z data out

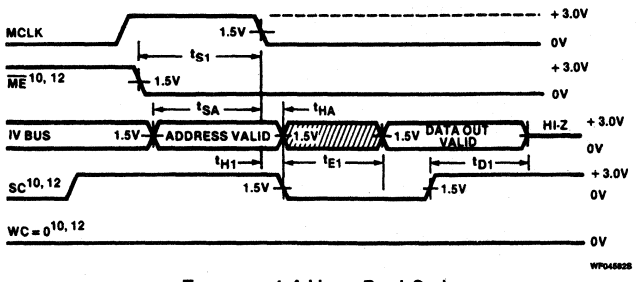
NOTE:
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

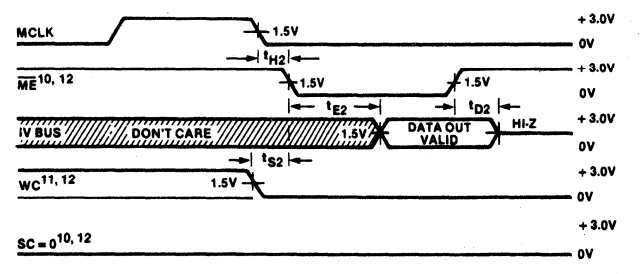
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Enable time							
t_{E1}	Output	Data out	$\overline{SC}$–			35	ns
t_{E2}	Output	Data out	$\overline{ME}$–			35	
Disable time[13]							
t_{D1}	Output	Data out	$\overline{SC}$+			35	ns
t_{D2}	Output	Data out	$\overline{ME}$+			35	
Pulse width[8]							
t_W	Master clock			40			ns
Setup and hold time							
t_{SA}	Setup time	MCLK–	Address	30			ns
t_{HA}	Hold time	Address	MCLK–	5			
t_{SD}	Setup time	MCLK–	Data in	35			
t_{HD}	Hold time	Data in	MCLK–	5			
t_{S3}	Setup time	MCLK–	$\overline{ME}$–	40			
t_{H3}	Hold time	$\overline{ME}$+	MCLK–	5			
t_{S1}	Setup time	MCLK–	$\overline{ME}$–	30			
t_{H2}	Hold time	$\overline{ME}$–	MCLK–	5			
t_{S2}	Setup time	$\overline{ME}$–	SC–, WC–	0			
t_{H1}	Hold time	SC–	MCLK–	5			
t_{H4}	Hold time	WC–	MCLK–	5			

NOTES:
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
3. Test each pin one at a time.
4. Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic High stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
10. SC + ME = 1 to avoid bus conflict.
11. WC + ME = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X300 are never at 1 simultaneously.
13. Measured at at delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 500\Omega$, and $C_L = 5pF$.

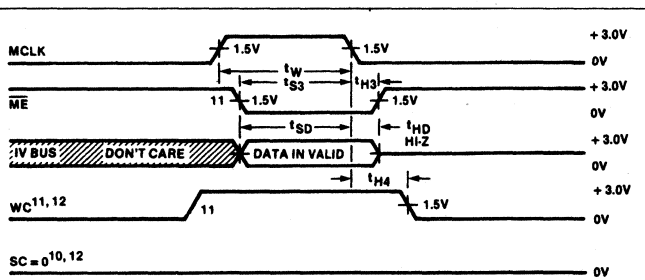
TIMING DIAGRAMS



Transparent Address Read Cycle



Latched Address Read Cycle



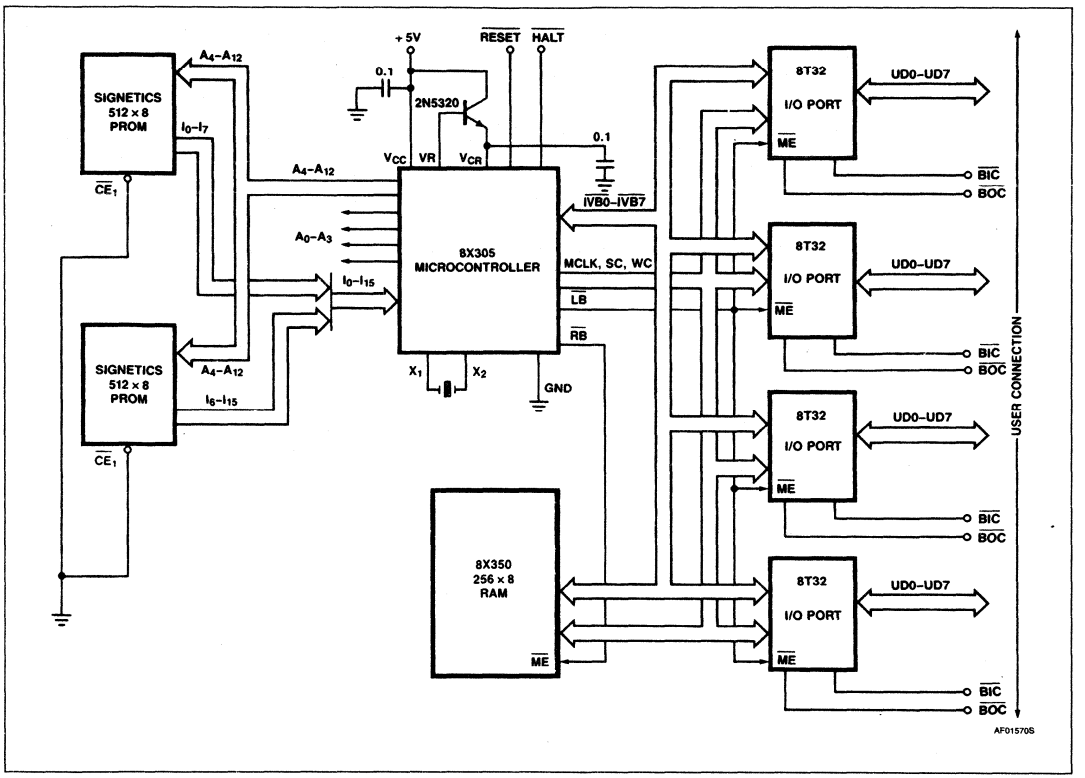
Latched Address Write Cycle

MEMORY TIMING DEFINITIONS

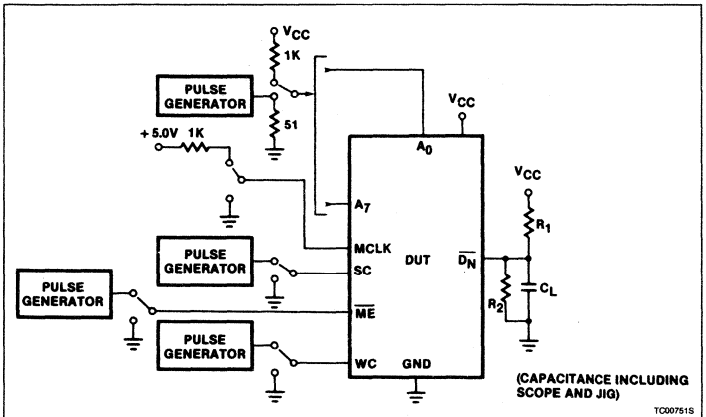
t_{S1}	Required delay between beginning of Master Enable Low and falling edge of Master Clock.
t_{SA}	Required delay between beginning of valid Address and falling edge of Master Clock.
t_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
t_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes Low.
t_{E1}	Delay between beginning of Select Command Low and beginning of valid Data Output on the IV Bus.
t_{D1}	Delay between when Select Command becomes High and end of valid Data Output on the IV Bus.
t_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes Low.
t_{E2}	Delay between when Master Enable becomes Low and beginning of valid Data Output on the IV Bus.
t_{D2}	Delay between when Master Enable becomes High and end of valid Data Output on the IV Bus.
t_{S2}	Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
t_W	Minimum width of the Master Clock pulse.
t_{S3}	Required delay between when Master Enable becomes Low and falling edge of Master Clock.
t_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes High.
t_{SD}	Required delay between beginning of valid Data Input on the IV Bus and falling edge of Master Clock.
t_{HD}	Required delay between falling edge of Master Clock and end of valid Data Input on the IV Bus.
t_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes Low.

2K-Bit TTL Bipolar RAM (256 × 8) — 8X350

TYPICAL 8X350 APPLICATION



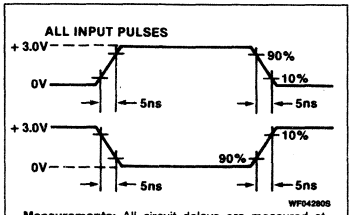
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

Loading Condition

VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the+1.5V level of inputs and output.

Input Pulses

PROM Programming Information

Generic Programming Procedures

GENERIC I PROGRAMMING

The Signetics family of Advanced Junction Isolated Schottky PROMs are high performance bipolar devices which use a nickel/chromium (NiCr) alloy fuse to provide the many benefits of field programming. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming (except the 82S115 which has two fusing pins: FE1 and FE2). The programming voltages and timing requirements make unintentional programming virtually impossible. Arrays of devices may be programmed in the user's circuit, if desirable, as long as proper application of programming voltages is provided.

GENERIC I PROCEDURE

The Generic I family of Schottky PROMs uses no special pins for programming. The address pins remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{CC} pin to 8.75 ± 0.25V. This voltage is referred to as V_{CCP}. After the proper delay the output corresponding to the bit selected is raised to 17.5 ± 0.5V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF} is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 10 to 25μs. It is during this time that the actual fusing of the NiCr link occurs. The actual time for fusing of a Signetics NiCr fuse link has been determined to be between 0.6 to 1.2μs. The shorter the fusing pulse (CE), within the recommended limits, the sooner the total programming sequence is completed. Note that unprogrammed Generic I (Junction Isolated) parts are supplied with all bits at a logic "0" level. Only the bits intended to be "ones" will be programmed. Verification of programming can be performed after each bit or after the entire device has been programmed.

A fuse which does not blow during the first programming cycle should be considered a defective device and should be discarded.

GENERIC II PROGRAMMING

The Signetics family of Oxide Isolated Schottky PROMs are high performance bipolar devices which use a vertical diode fuse to provide the benefits of field programming. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming. The programming voltages and timing requirements make unintentional programming virtually impossible.

GENERIC II PROCEDURE

As with the Generic I devices, the addresses remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{CC} pin to 8.75 ± 0.25V. This voltage is referred to as V_{CCP}. After the proper delay the output corresponding to the bit selected is raised to 20.0 ± 0.5V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF} is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 1μs. The properly blown fuse will verify the TTL "0" level. Note that unprogrammed Generic II (Oxide Isolated) parts are supplied with all bits at a logic "1" level. Only the bits intended to be "zeros" will be programmed.

PROGRAMMING INFORMATION

Complete programming system specifications for both Generic I and Generic II products are available upon request from Bipolar Memory Marketing.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available on request from Bipolar Memory Marketing.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT.

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Records of programming yield, by device type, should be kept and any downward trend or sudden change should be considered as an indication of a need to recalibrate the programming equipment.

Low Complexity PROM

Signetics

82S23
82S123
256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following pages.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

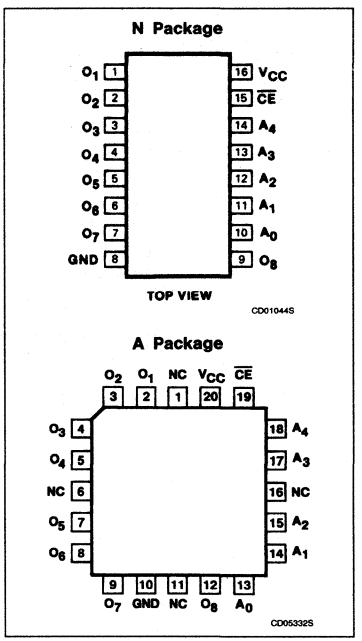
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S23: Open Collector**
  - **N82S123: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

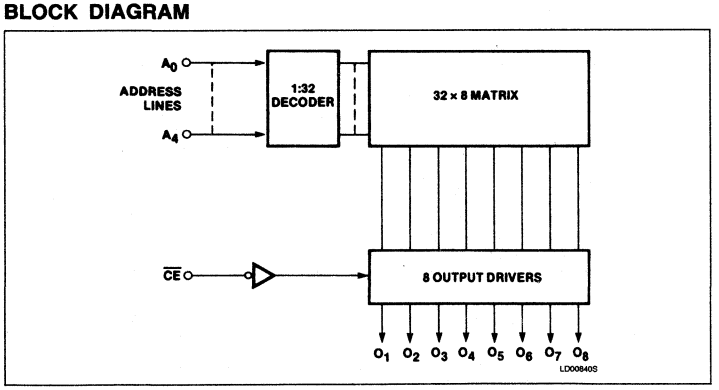
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8) — 82S23, 82S123

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S23 N • N82S123 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S23 A • N82S123 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S23) Off-state (82S123)	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

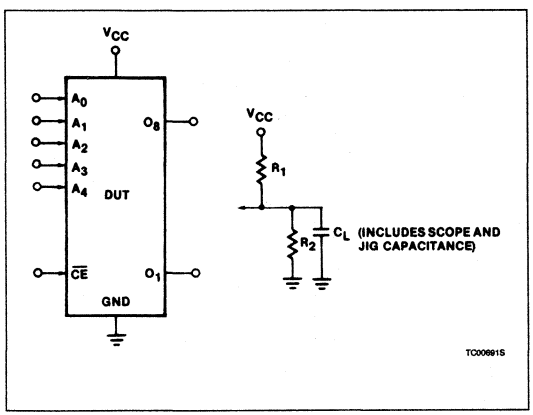
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			
V_{IC}	Clamp	I_{IN} = −12mA			−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			50	
Output current						
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S123)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			96	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

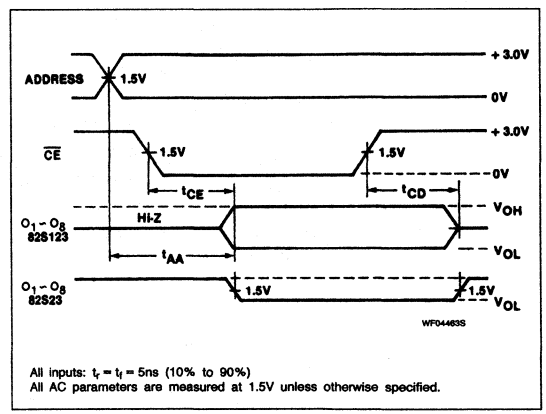
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		45	50	ns
t_{CE}		Output	Chip enable			35	ns
Disable time[6]							
t_{CD}		Output	Chip enable			35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S23A
82S123A
256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23A and 82S123A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23A and 82S123A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S23A and 82S123A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

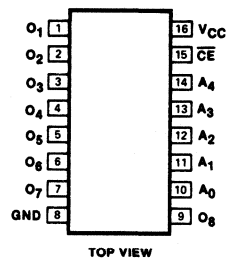
- **Address access time: 25ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S23A: Open Collector**
  - **N82S123A: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

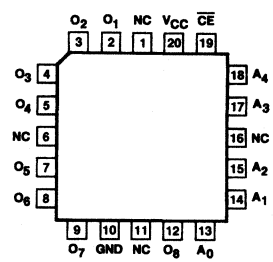
N Package



TOP VIEW

CD01044S

A Package



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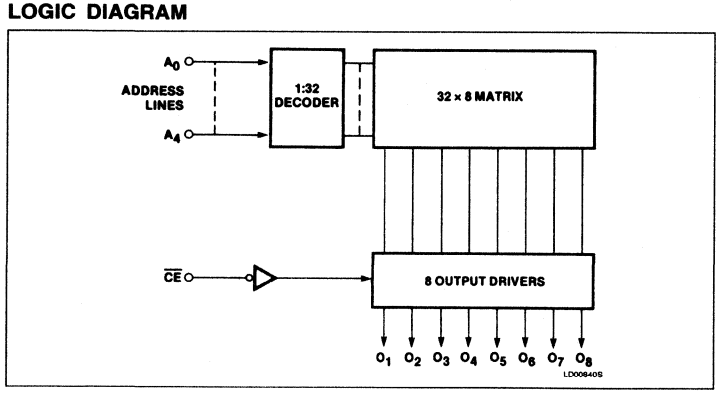
LOGIC DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8) — 82S23A, 82S123A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S23A N • N82S123A N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S23A A • N82S123A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S23A) Off-state (82S123A)	 +5.5 +5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	 0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

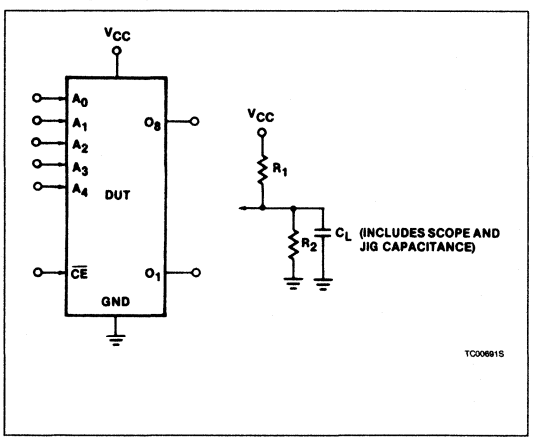
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			50	
Output current						
I_{OLK}	Leakage (82S23A)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82S123A)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82S123A)[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			96	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

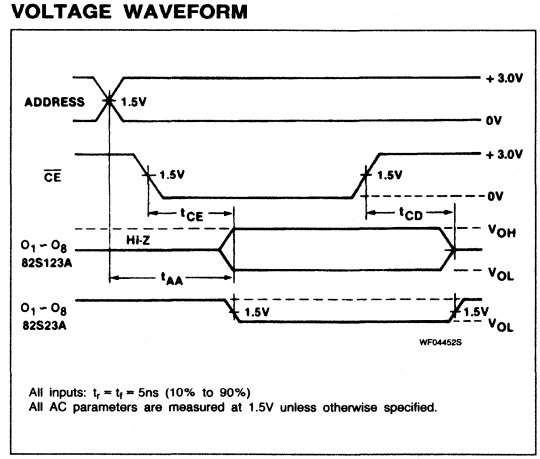
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time							
t_{AA}[4]		Output	Address		20	25	ns
t_{CE}		Output	Chip enable			18	ns
Disable time[6]							
t_{CD}		Output	Chip disable			18	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82US23
82US123
256-Bit TTL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 82US23 and 82US123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82US23 and 82US123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ti-W link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82US23 and 82US123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

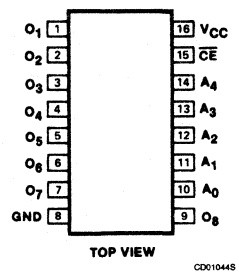
- **Address access time: 10ns max**
- **Power dissipation: 2.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82US23: Open Collector**
  - **N82US123: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

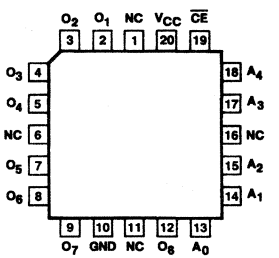
N Package



TOP VIEW

CD01044S

A Package



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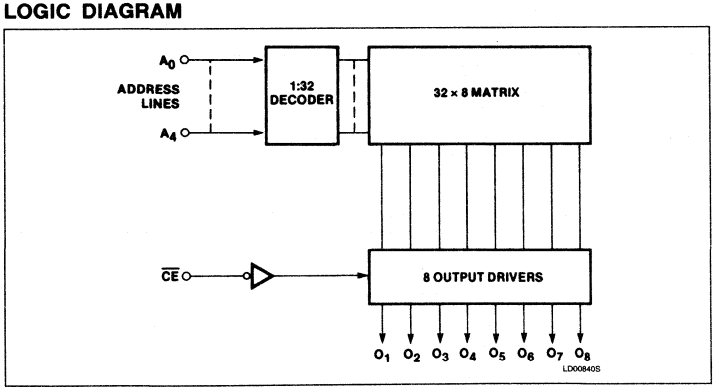
LOGIC DIAGRAM



LD00840S

256-Bit TTL Bipolar PROM (32 × 8) — 82US23, 82US123

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82US23 N • N82US123 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82US23 A • N82US123 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
	Output voltage		
V_{OH}	High (82US23)	+5.5	V_{DC}
V_O	Off-state (82US123)	+5.5	
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$			−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.5V$			50	
Output current						
I_{OLK}	Leakage (82US23)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82US123)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82US123)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			115	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

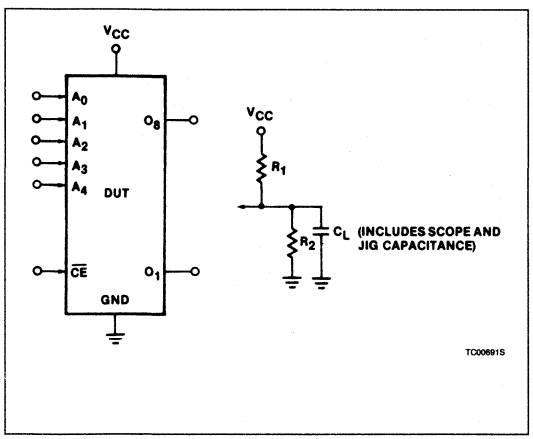
256-Bit TTL Bipolar PROM (32 × 8) — 82US23, 82US123

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

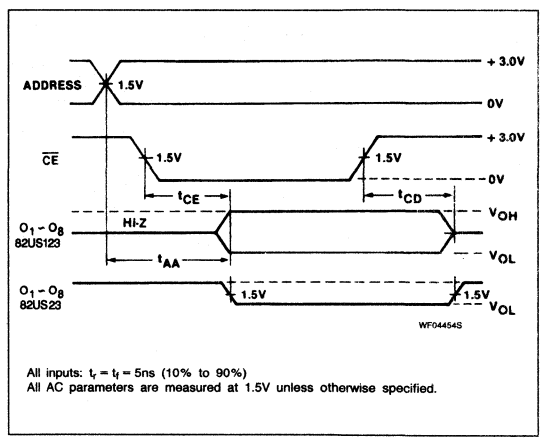
SYMBOL	PARAMETER	TO	FROM	N82US23			N82US123			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address			13			10	ns
t_{CE}		Output	Chip enable			8			7	ns
Disable time[6]										
t_{CD}		Output	Chip enable			8			7	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S126
82S129
1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

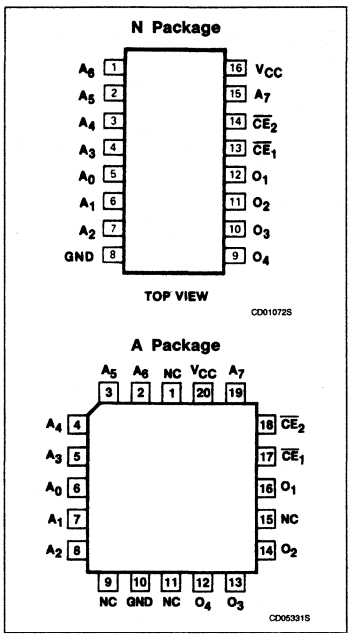
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Two Chip Enable inputs**
- **Output options:**
  - **N82S126: Open Collector**
  - **N82S129: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

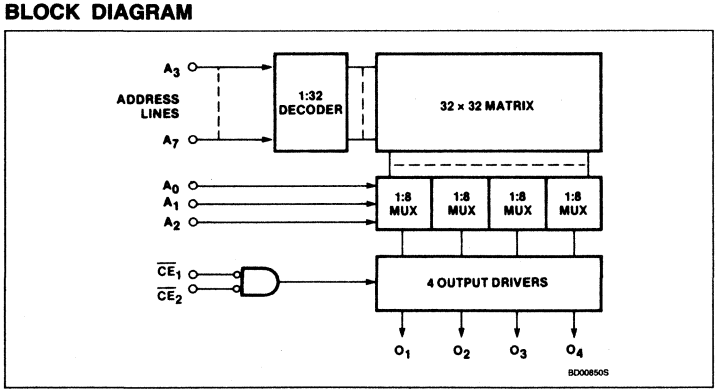
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



1K-Bit TTL Bipolar PROM (256 × 4) — 82S126, 82S129

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S126 N • N82S129 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S126 A • N82S129 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S126) Off-state (82S129)	 +5.5 +5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	 0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

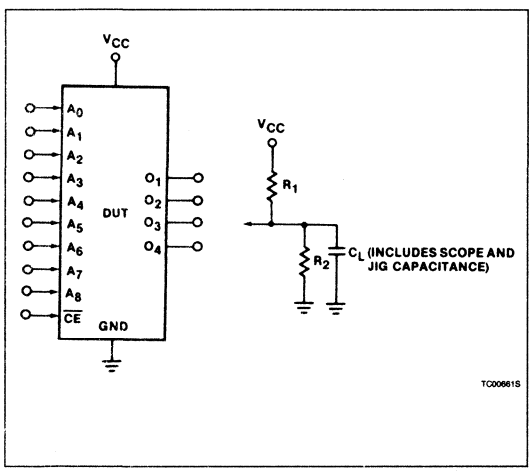
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
V_{OL}	Low	$\overline{CE}_{1,2}$ = Low I_{OUT} = 16mA			0.45	V
V_{OH}	High (82S129)	$I_{OUT} = -2.0mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82S129)[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			120	mA
Capacitance						
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

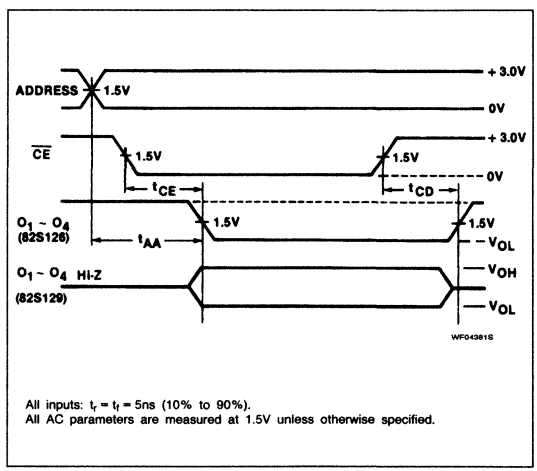
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	50	ns
t_{CE}		Output	Chip enable			25	ns
Disable time[6]							
t_{CD}		Output	Chip disable			25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S126A
82S129A
1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126A and 82S129A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126A and 82S129A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126A and 82S129A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

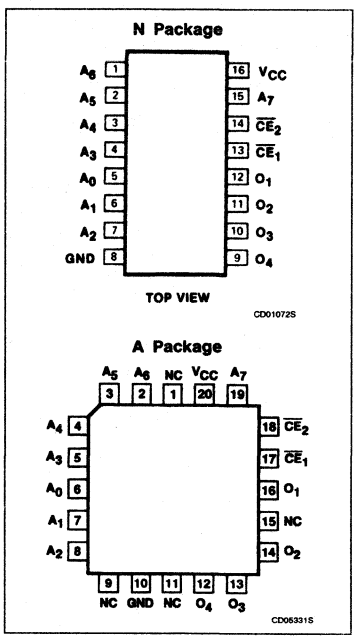
FEATURES

- **Address access time:**
  - **N82S126A: 30ns max**
  - **N82S129A: 27ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Two Chip Enable inputs**
- **Output options:**
  - **82S126A: Open Collector**
  - **82S129A: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

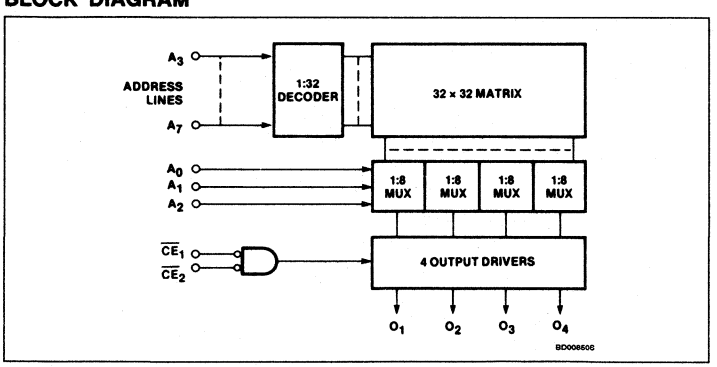
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



1K-Bit TTL Bipolar PROM (256 × 4) — 82S126A, 82S129A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S126A N • N82S129A N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S126A A • N82S129A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
	Output voltage		
V_{OH}	High (82S126)	+5.5	V_{DC}
V_O	Off-state (82S129)	+5.5	
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			
V_{IC}	Clamp	V_{CC} = 4.75V, I_{IN} = −12mA			−1.2	
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High (82S129A)	I_{OUT} = −2.0mA	2.4			
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current						
I_{OLK}	Leakage (82S126A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S129A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S129A)[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			120	mA
Capacitance						
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

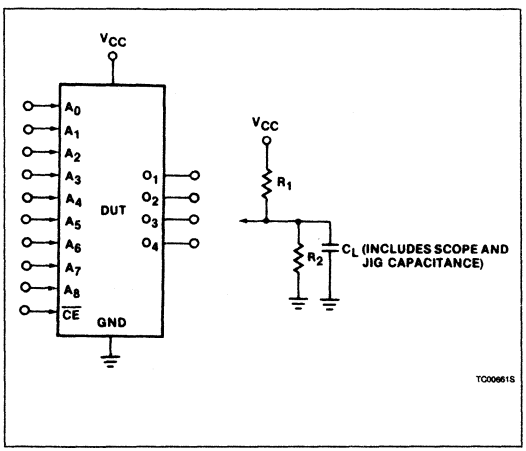
1K-Bit TTL Bipolar PROM (256 × 4) — 82S126A, 82S129A

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

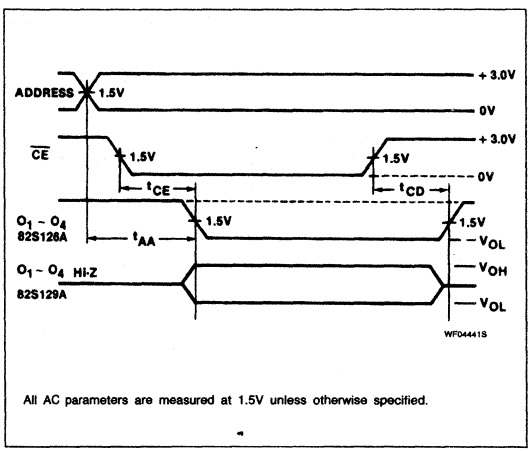
SYMBOL	PARAMETER	TO	FROM	N82S129A			N82S126A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		17	27		17	30	ns
t_{CE}		Output	Chip enable		10	20		10	20	ns
Disable time[6]										
t_{CD}		Output	Chip enable		6	15		6	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S130
82S131
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130 and 82S131 are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S130 and 82S131 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

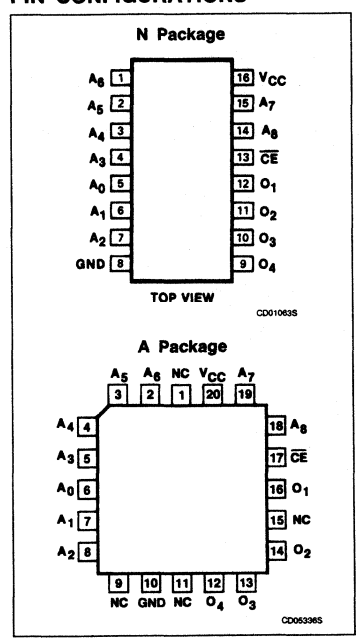
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S130: Open Collector**
  - **N82S131: 3-State**
- **No separate fusing-pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

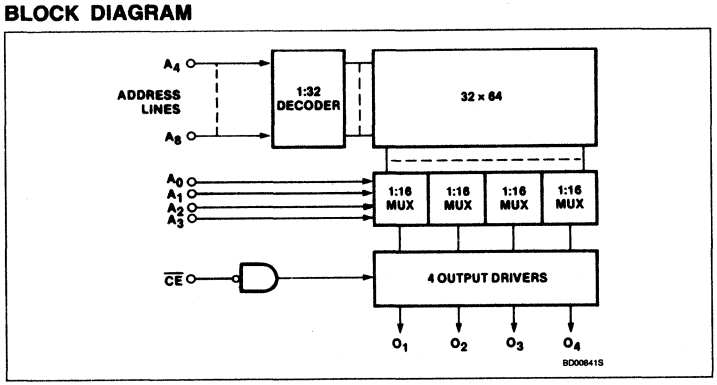
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (512 × 4) — 82S130, 82S131

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S130 N • N82S131 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S130 A • N82S131 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
	Output voltage		
V_{OH}	High (82S130)	+5.5	V_{DC}
V_O	Off-state (83S131)	+5.5	
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

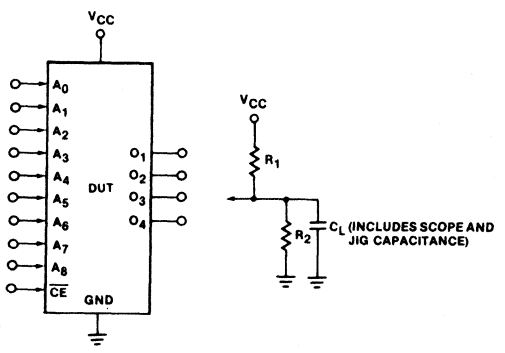
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low			0.8		V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High (82S131)	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$,			40	μA
I_{OZ}	Hi-Z State (82S131)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82S131)[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			140	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address			50	ns
t_{CE}		Output	Chip enable			30	ns
Disable time[6]							
t_{CD}		Output	Chip disable			30	ns

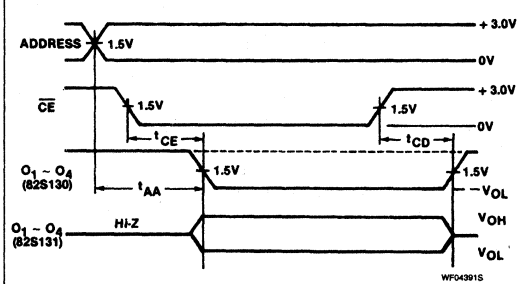
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

Signetics

82S130A
82S131A
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S130A and 82S131A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130A and 82S131A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S130A and 82S131A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

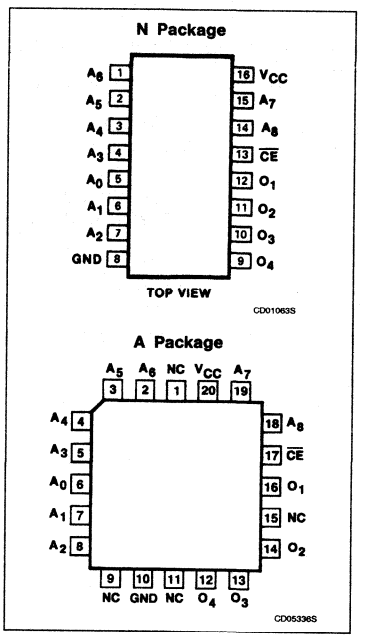
FEATURES

- **Address access time:**
  - **N82S130A: 33ns max**
  - **N82S131A: 30ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S130A: Open Collector**
  - **N82S131A: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

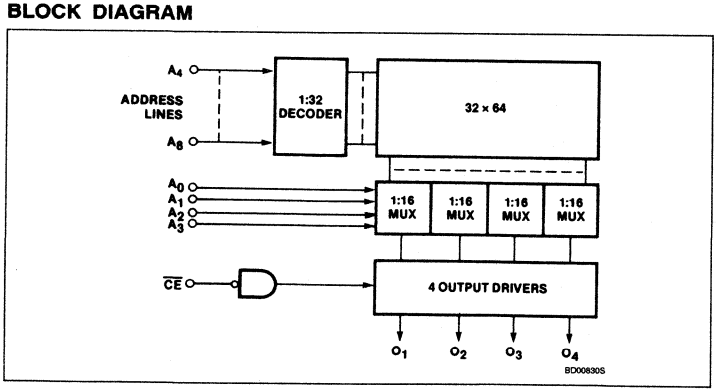
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (512 × 4) — 82S130A, 82S131A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S130A N • N82S131A N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S131A A • N82S131A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S130) Off-state (82S131)	 +5.5 +5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	 0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

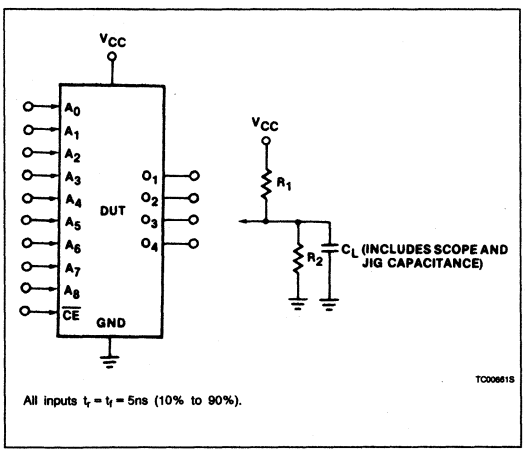
SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High (82S131)	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OLK}	Leakage (82S130A)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82S131A)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82S131A)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			140	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S131A			N82S130A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		18	30		18	33	ns
t_{CE}		Output	Chip enable		10	20		10	20	ns
Disable time[6]										
t_{CD}		Output	Chip enable		6	15		6	15	ns

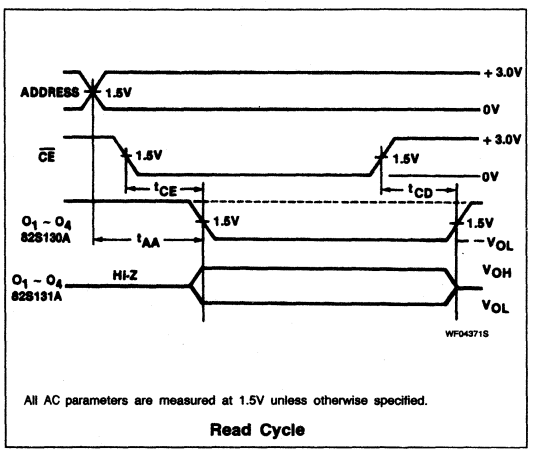
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

Signetics

82S135
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S135 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

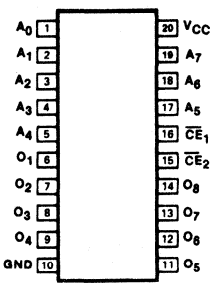
- **Address access time: 45ns max**
- **Power dissipation: 329μW/bit typ**
- **Input loading: −100μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **Unprogrammed outputs are Low level**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

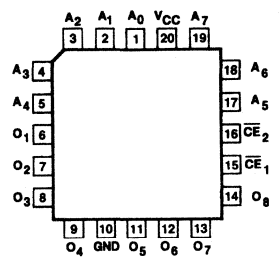
N Package



TOP VIEW

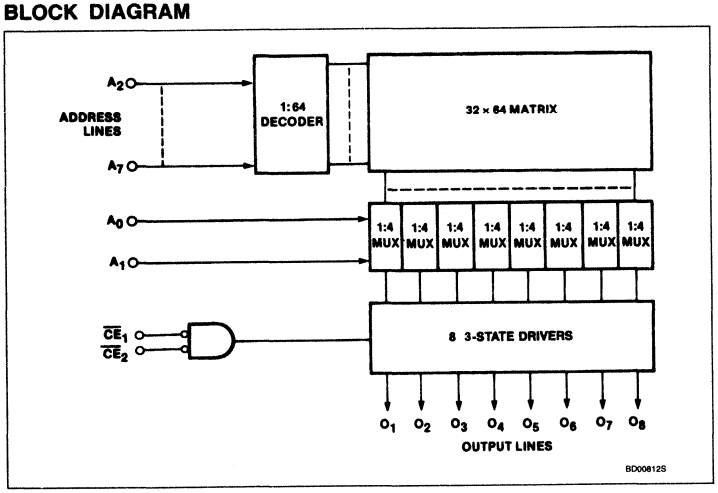
CD01033S

A Package



CD05337S

BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (256 × 8) — 82S135

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82S135 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S135 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL} V_{IH} V_{IC}	Low High Clamp	V_{CC} = 4.75V V_{CC} = 5.25V I_{IN} = −12mA	2.0		0.8 −1.2	V
Output voltage						
V_{OL} V_{OH}	Low High	I_{OUT} = 9.6mA $\overline{CE}_1$, $\overline{CE}_2$ = Low, I_{OUT} = −2mA, High stored	2.4		0.5	V
Input current						
I_{IL} I_{IH}	Low High	V_{IN} = 0.45V V_{IN} = 5.5V			−100 40	μA
Output current						
I_{OZ} I_{OS}	Hi-Z State Short circuit[3]	$\overline{CE}_1$, $\overline{CE}_2$ = High, V_{OUT} = 0.5V $\overline{CE}_1$, $\overline{CE}_2$ = High, V_{OUT} = 5.5V $\overline{CE}_1$, $\overline{CE}_2$ = Low, V_{OUT} = 0V, High stored	−15		−40 40 −75	μA mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		135	150	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	V_{CC} = 5.0V, $\overline{CE}$ = High V_{IN} = 2.0V V_{OUT} = 2.0V		5 8		pF

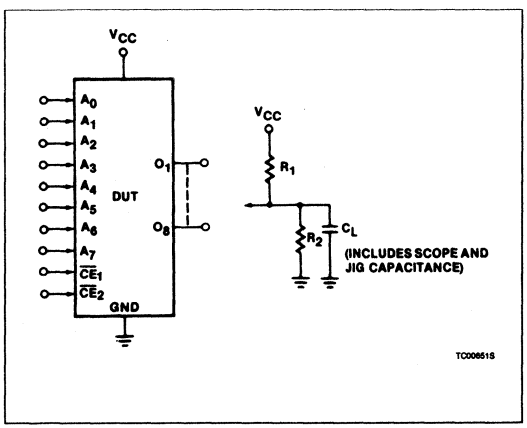
2K-Bit TTL Bipolar PROM (256 × 8) — 82S135

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

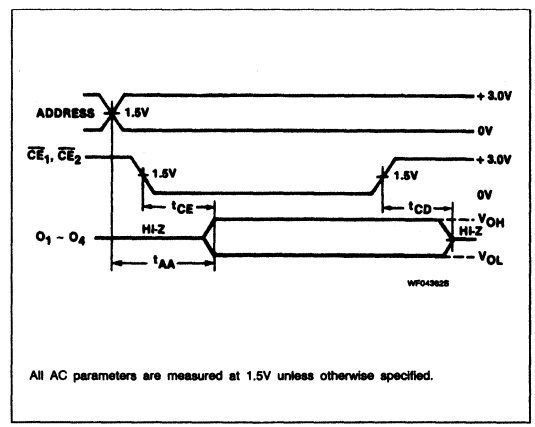
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	45	ns
t_{CE}		Output	Chip enable		20	25	ns
Disable time[6]							
t_{CD}		Output	Chip disable		20	35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82LS135
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

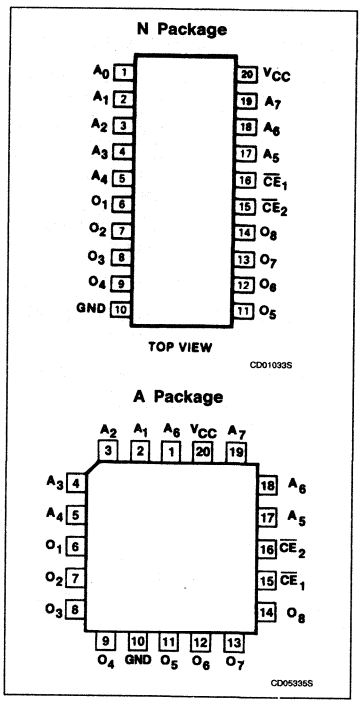
FEATURES

- **Address access time: 100ns max**
- **Power dissipation: 200μW/bit typ**
- **Input loading: −100μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Unprogrammed outputs are at Low level**
- **Outputs: 3-State**

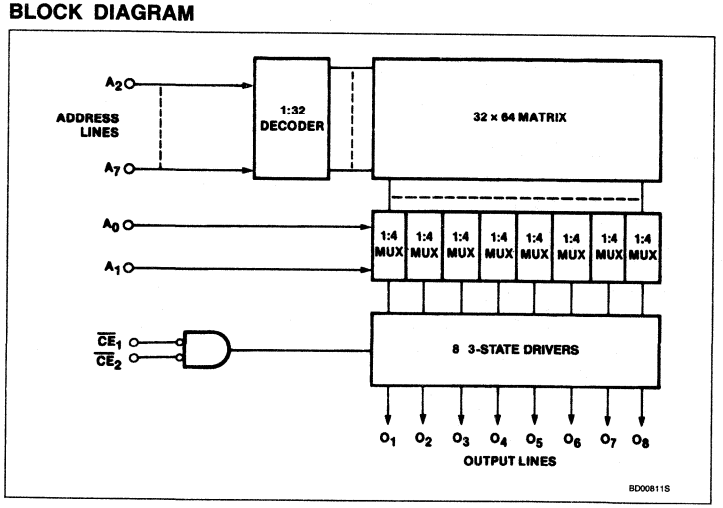
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (256 × 8) — 82LS135

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82LS135 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82LS135 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
	Temperature Range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$, High stored	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IH} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$, $\overline{CE}_2$ = Low, $V_{OUT} = 0V$, High stored	−15		−75	ma
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		80	100	mA
Capacitance						
		$V_{CC} = 5.0V$, $\overline{CE}$ = High				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

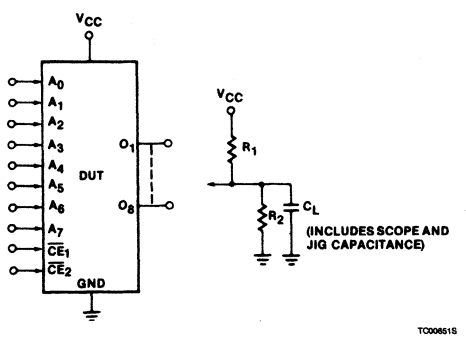
2K-Bit TTL Bipolar PROM (256 × 8) — 82LS135

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip enable		30	50	ns
Disable time[6]							
t_{CD}		Output	Chip disable		30	60	ns

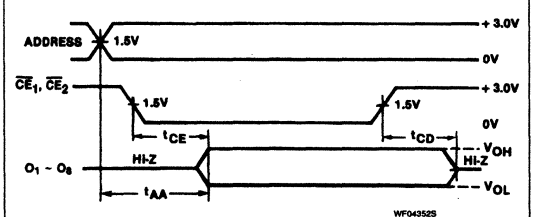
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

VOLTAGE WAVEFORM



4K-bit TTL Bipolar PROM

Signetics

82S115
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the 3-State output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of Address or Chip Enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

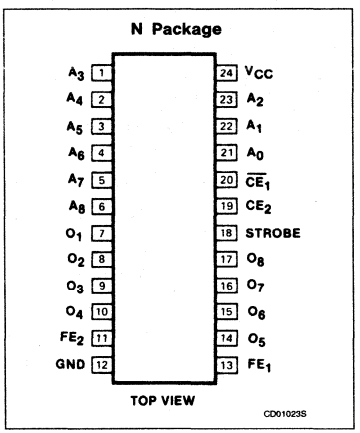
FEATURES

- **Address access time: 60ns max**
- **Power dissipation: 165μW/bit typ**
- **Input loading: −100μA max**
- **Two Chip Enable inputs**
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**
- **Outputs: 3-State**

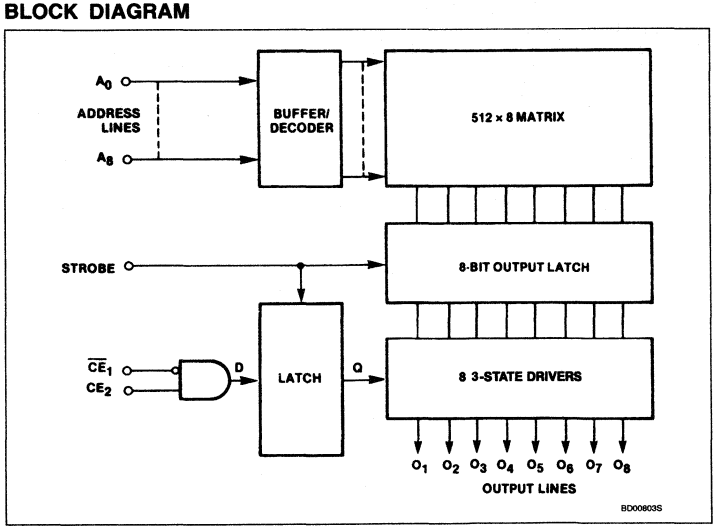
APPLICATIONS

- **Microprogramming**
- **Hardware algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (512 × 8) — 82S115

ORDERING INFORMATION

DESCRIPTION	ORDERING CODE
24-pin Plastic DIP 600mil-wide	N82S115 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[5]	LIMITS			UNIT
			Min	Typ[6]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$		0.4	0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.7			
Input current[5]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			25	
Output current[5]						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High or CE_2 = Low, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}_1$ = High or CE_2 = Low, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[1]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$, High stored	−15		−70	mA
Supply current[10]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High or CE_2 = Low, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

4K-Bit TTL Bipolar PROM (512 × 8) — 82S115

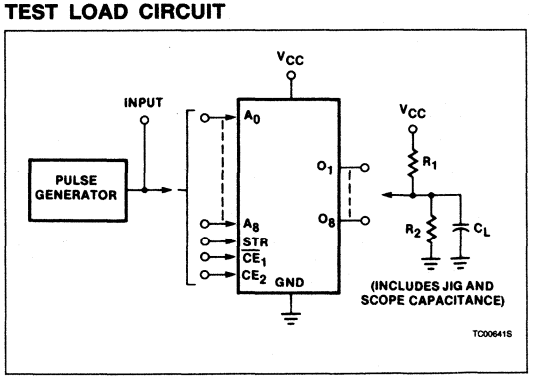
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[8]	Max	
Access time[6]								
t_{AA} t_{CE}		Output Output	Address Chip enable	Latched or transparent Read[2,4]		40 20	60 40	ns
Disable time[9]								
t_{CD}		Output	Chip disable	Latched or transparent Read[2,4]		20	40	ns
Setup and hold time								
t_{CDS} t_{CDH}	Setup time Hold time	Output	Chip enable	Latched Read only[3,4]	40 10			ns
Hold time								
t_{ADH}	Hold time	Address	Strobe	Latched Read only[3,4]		0		ns
Pulse Width								
t_{SW}	Strobe			Latched Read only[3,4]	30	15		ns
Latch time								
t_{SL}	Strobe			Latched Read only[3,4]	60	35		ns
Delatch time[9]								
t_{DL}	Strobe			Latched Read only[3,4]			35	ns

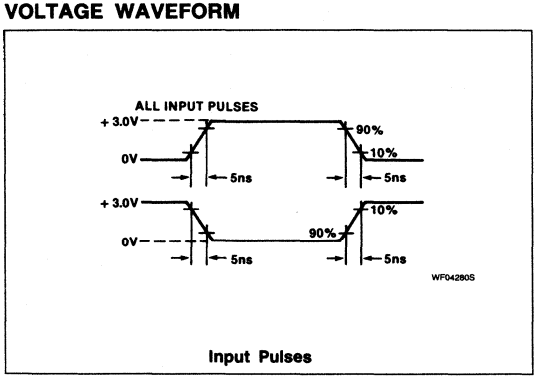
NOTES:

1. No more than one output should be grounded at the same time and strobe should be disabled Strobe is in the High state.
2. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed or T_{CE} nanoseconds after the output circuit is enabled.
3. In latched Read Mode data from any selected address will be held on the output when Strobe is lowered only when Strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
4. During operation the fusing pins FE_1 and FE_2 must be grounded or left floating.
5. Positive current is defined as into the terminal referenced.
6. Tested at an address cycle time of 1μs.
7. Areas shown by crosshatch are latched data from previous address.
8. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
9. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, and $C_L = 5pF$.
10. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT

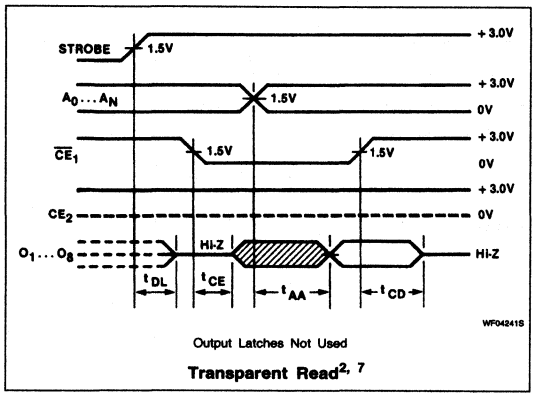


VOLTAGE WAVEFORM



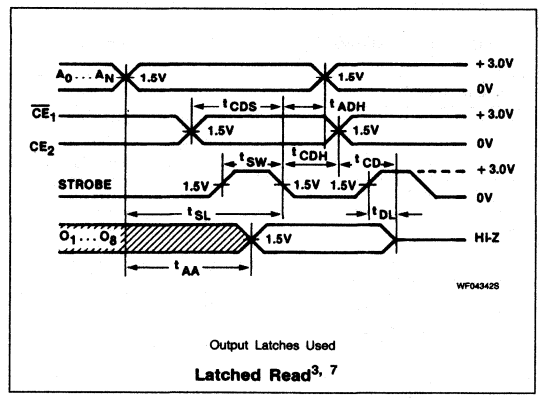
Input Pulses

TIMING DIAGRAMS



Output Latches Not Used

Transparent Read[2, 7]



Output Latches Used

Latched Read[3, 7]

Signetics

82S137
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137 devices are also processed to military requirements for operation over the military temperature range, for specifications and ordering information consult the Signetics Military Data Book.

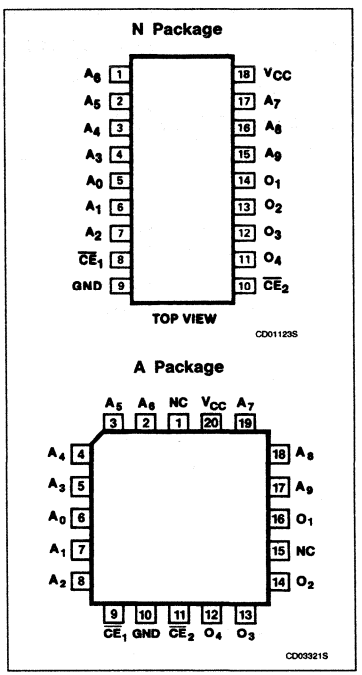
FEATURES

- **Address access time: 60ns max**
- **Power dissipation: 0.13mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Two Chip Enable inputs**
- **Outputs: 3-State**

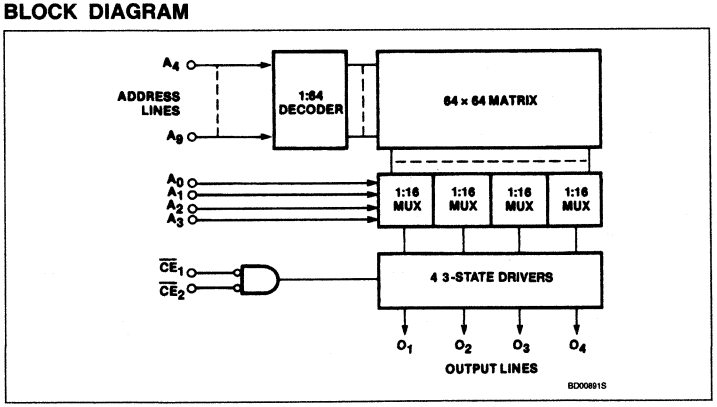
APPLICATIONS

- **Sequential controllers**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S137 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S137 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_{1,2}$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $V_{OUT} = 0V$, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			140	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

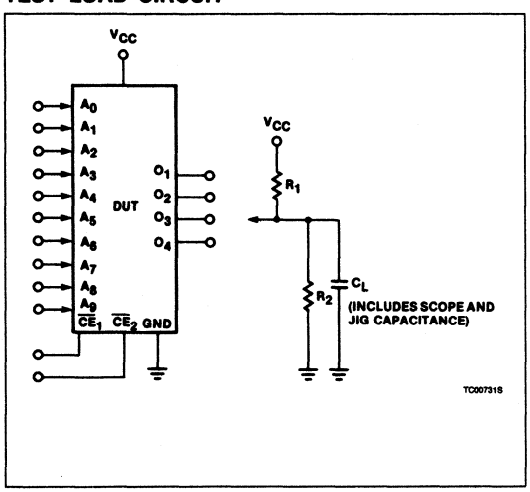
4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

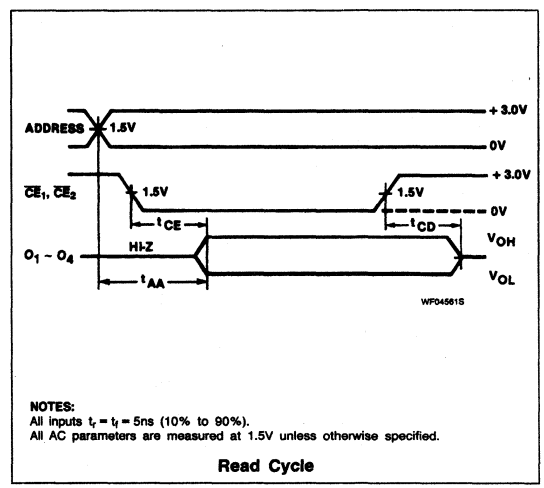
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	60	ns
t_{CE}		Output	Chip enable		25	30	ns
Disable time[6]							
t_{CD}		Output	Chip enable		25	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

Signetics

82S137A
82S137B
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S137A and 82S137B are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137A and 82S137B are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

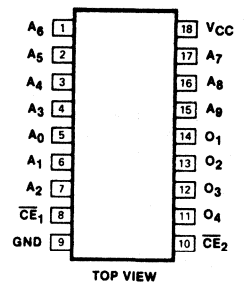
- **Address access time:**
  - **N82S137A: 45ns max**
  - **N82S137B: 35ns max**
- **Power dissipation: 0.13mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Two Chip Enable inputs**
- **Outputs: 3-State**

APPLICATIONS

- **Control store**
- **Sequential controllers**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

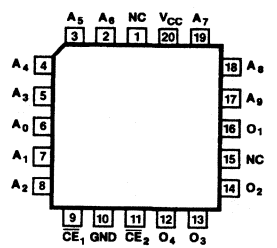
N Package



TOP VIEW

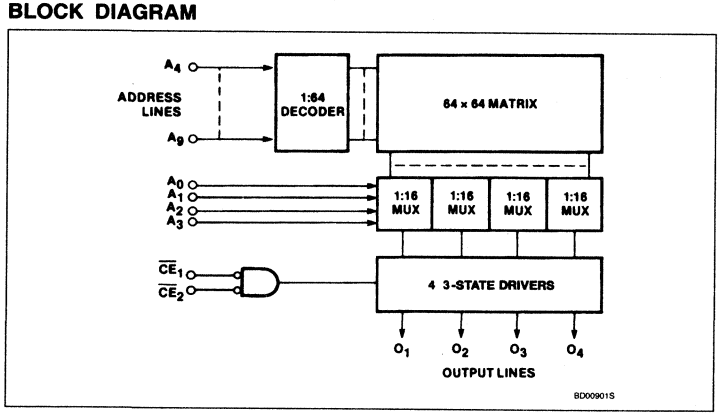
CD01142S

A Package



CD03321S

BLOCK DIAGRAM



BD00901S

4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137A, 82S137B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S137A N • N82S137B N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S137A A • N82S137B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature Range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

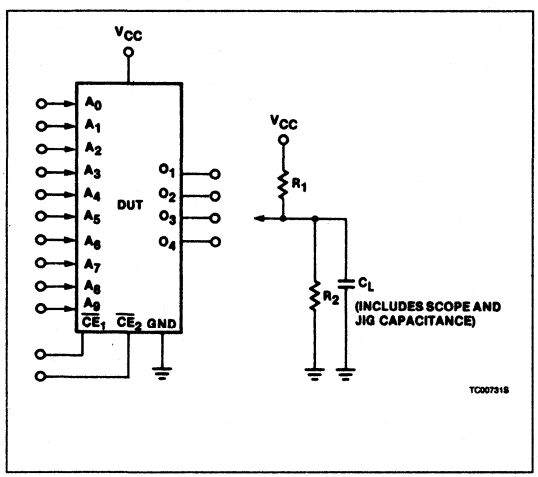
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL} V_{IH} V_{IC}	Low High Clamp	 $I_{IN} = -12mA$	 2.0 	 −0.8	0.8 −1.2	V
Output voltage						
V_{OL} V_{OH}	Low High	$\overline{CE}_{1,2}$ = Low $I_{OUT} = 16mA$ $I_{OUT} = -2mA$	 2.4		0.45	V
Input current						
I_{IL} I_{IH}	Low High	$V_{IN} = 0.45V$ $V_{IN} = 5.5V$			−100 40	μA
Output current						
I_{OZ} I_{OS}	Hi-Z State Short circuit[3]	$\overline{CE}_{1,2}$ = High, $V_{OUT} = 0.5V$ $\overline{CE}_{1,2}$ = High, $V_{OUT} = 5.5V$ $\overline{CE}_{1,2}$ = Low, $V_{OUT} = 0V$ High stored	 −15		40 −40 −70	μA mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		85	140	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$ $V_{OUT} = 2.0V$		5 8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

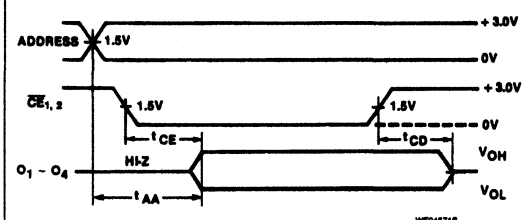
SYMBOL	PARAMETER	TO	FROM	N82S137A			N82S137B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		35	45		30	35	ns
t_{CE}		Output	Chip enable		20	30		15	25	ns
Disable time[6]										
t_{CD}		Output	Chip disable		20	30		15	25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S137C
4K-Bit TTL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 82S137C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137C is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137C devices are also processed to military requirements for operation over the military temperature range, for specifications and ordering information consult the Signetics Military Data Book.

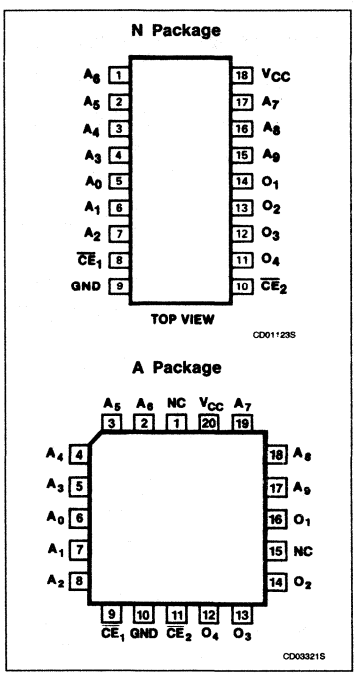
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.13mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Two Chip Enable inputs**
- **Outputs: 3-State**

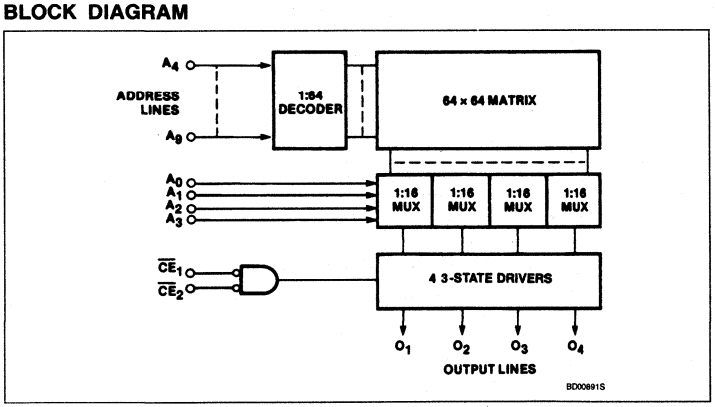
APPLICATIONS

- **Sequential controllers**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S137C N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S137C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, V_{OUT} = 0.5V			−40	μA
		$\overline{CE}_{1,2}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			140	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

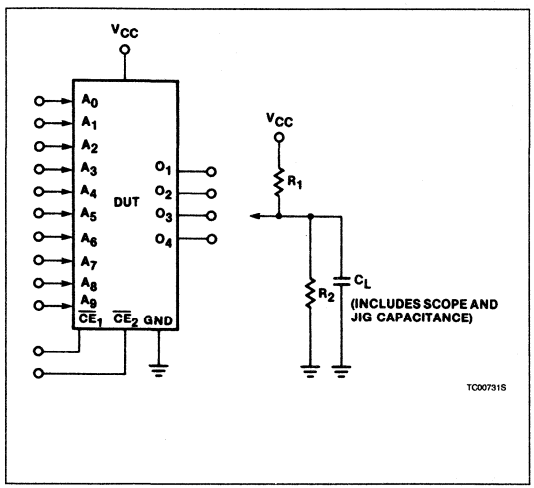
4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137C

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

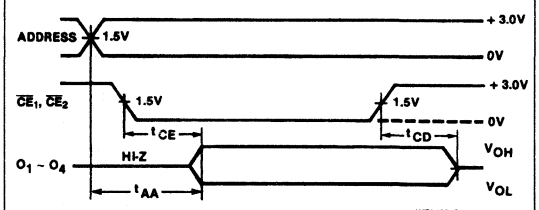
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address			20	ns
t_{CE}		Output	Chip enable			15	ns
Disable time[6]							
t_{CD}		Output	Chip enable			15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

Signetics

82S141
82S141A
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S141 and 82S141A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S141 and 82S141A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

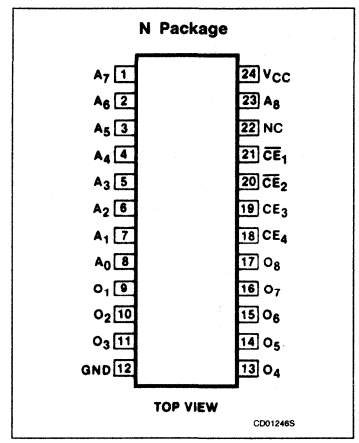
FEATURES

- **Address access time:**
  - **N82S141: 60ns max**
  - **N82S141A: 45ns max**
- **Power dissipation: 76μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Four Chip Enable inputs**
- **Outputs: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

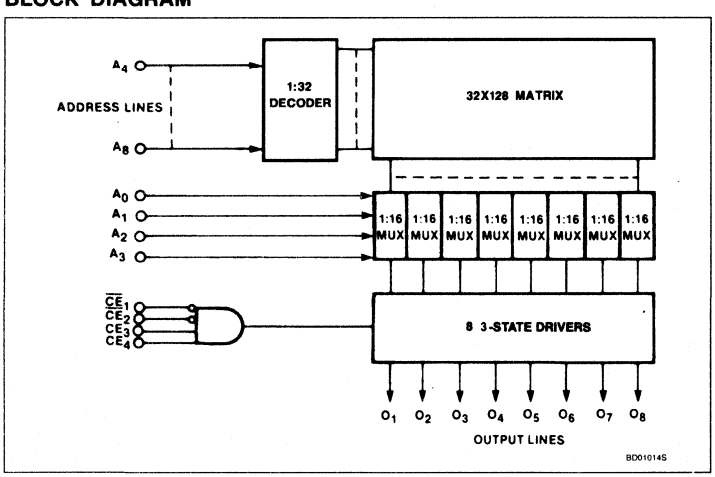
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (512 × 8) — 82S141, 82S141A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300 mil-wide	N82S141 N3 • N82S141A N3
24-pin Plastic DIP 600mil-wide	N82S141 N • N82S141A N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

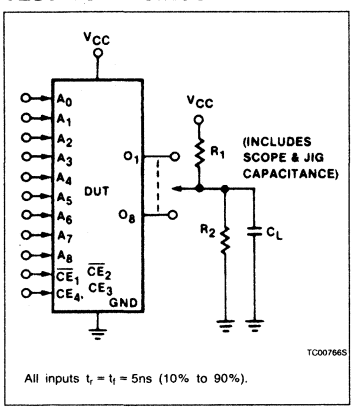
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage[2]						
V_{OL}	Low	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High $I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current[1]						
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$, $\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$			40 −40	μA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S141			N82S141A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address			60			45	ns
t_{CE}		Output	Chip Enable			40			30	ns
Disable time[6]										
t_{CD}		Output	Chip disable			40			30	ns

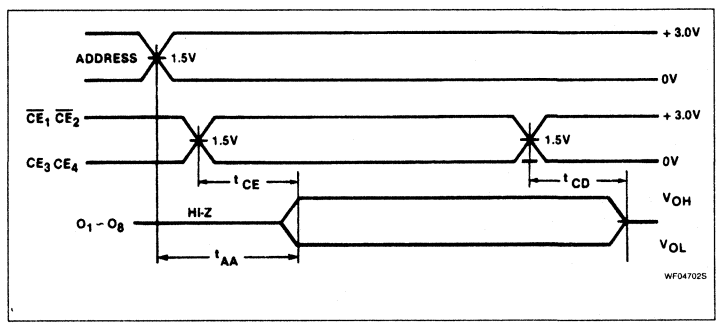
NOTES:
1. Positive current is defined as into the terminal referenced.
1. All voltages with respect to network ground.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORM



Signetics

82S147
82S147A
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S147 and 82S147A are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147 and 82S147A includes on-chip decoding and one Chip Enable input for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S147 and 82S147A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

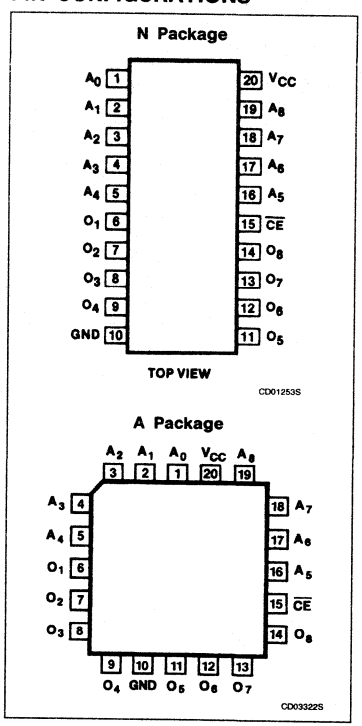
FEATURES

- **Address access time:**
  - **N82S147: 60ns max**
  - **N82S147A: 45ns max**
- **Power dissipation: 625mW typ**
- **Input loading: −100μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **Unprogrammed outputs are Low level**

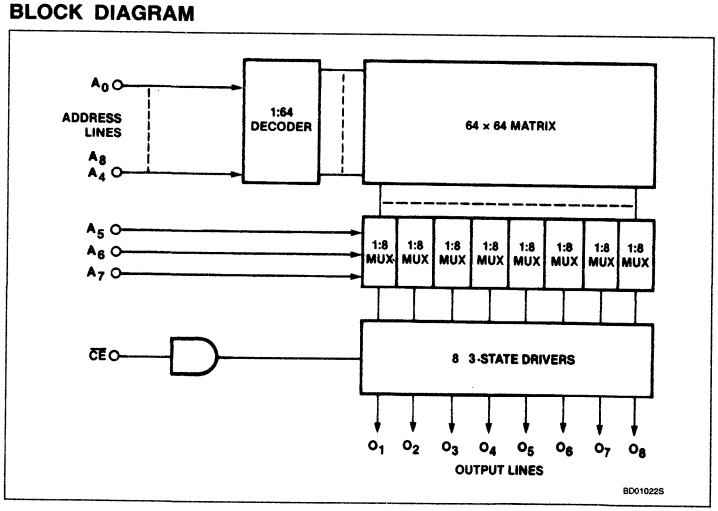
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



4K-Bit Bipolar PROM (512 × 8) — 82S147, 82S147A

ORDERING INFORMATION

PACKAGES	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82S147 N • N82S147A N
20-pin Plastic Leaded Chip Carrier 300mil-square	N82S147 A • N82S147A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

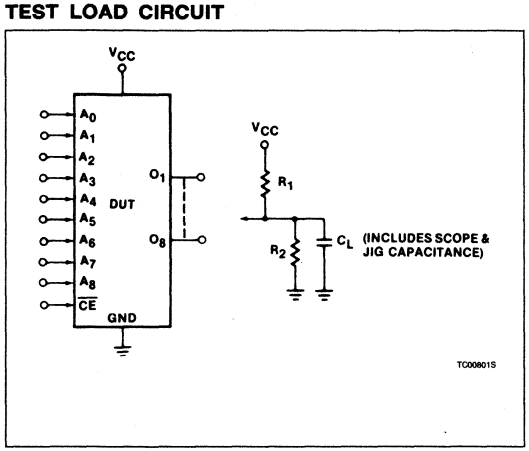
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	155	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

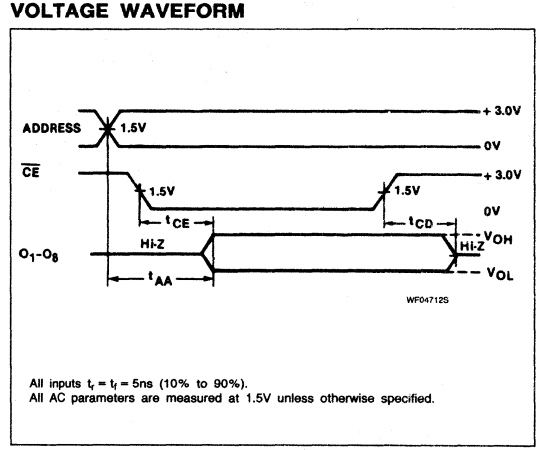
SYMBOL	PARAMETER	TO	FROM	N82S147			N82S147A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		45	60		40	45	ns
t_{CE}		Output	Chip Enable		20	35		20	30	ns
Disable time[6]										
t_{CD}		Output	Chip disable		20	35		20	30	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S147B
4K-Bit TTL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 82S147B is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147B includes on-chip decoding and one Chip Enable input for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S147B device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

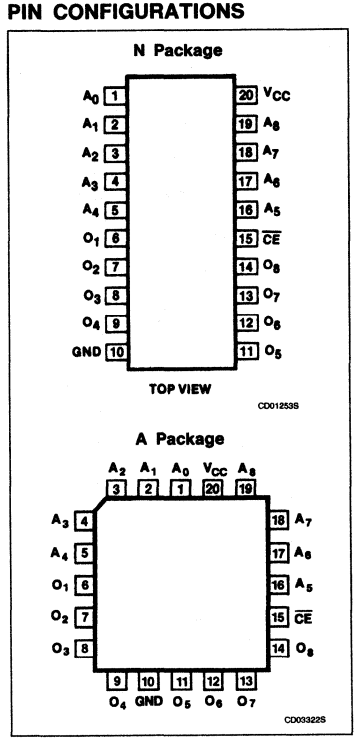
FEATURES

- **Address access time: 25ns max**
- **Power dissipation: 625mW typ**
- **Input loading: −100μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **Unprogrammed outputs are Low level**

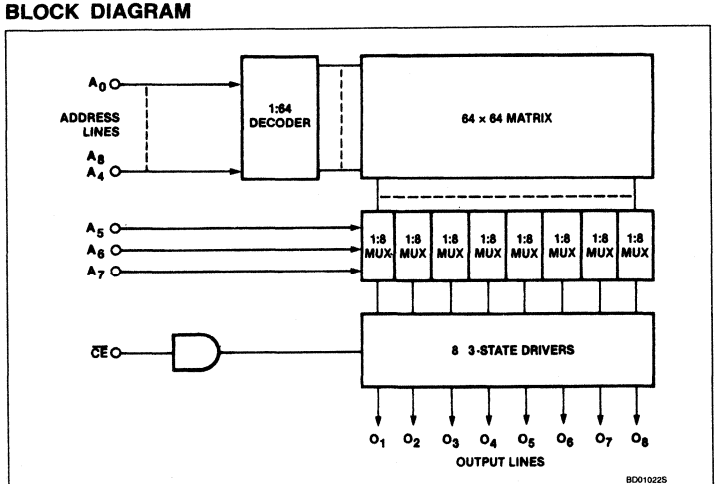
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



4K-Bit Bipolar PROM (512 × 8) — 82S147B

ORDERING INFORMATION

PACKAGES	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82S147B N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S147B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	155	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

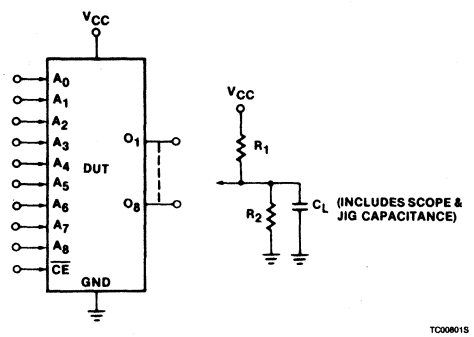
4K-Bit Bipolar PROM (512 × 8) — 82S147B

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

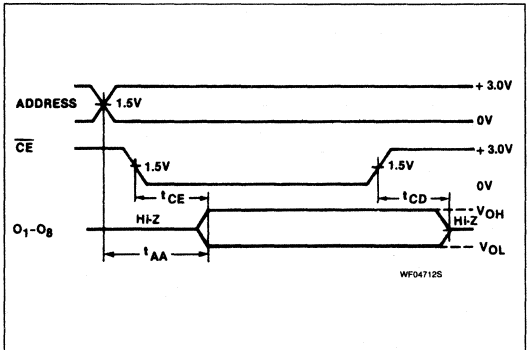
SYMBOL	PARAMETER	TO	FROM	N82S147B			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address			25	ns
t_{CE}		Output	Chip Enable			15	ns
Disable time[6]							
t_{CD}		Output	Chip disable			15	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

8K-bit TTL Bipolar PROM

Signetics

82S181
82S181A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S181 and 82S181A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181 and 82S181A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S181 and 82S181A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

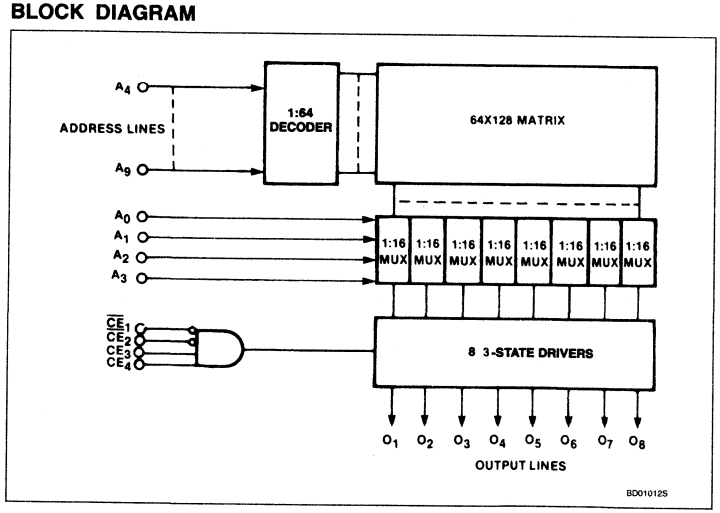
FEATURES

- **Address access time:**
  - **N82S181: 70ns max**
  - **N82S181A: 55ns max**
- **Power dissipation: 76μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Four Chip Enable inputs**
- **Outputs: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

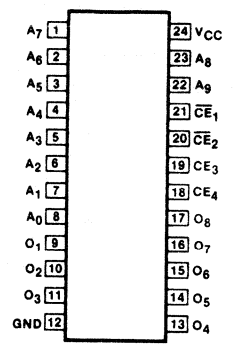
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATIONS

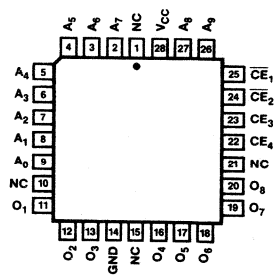
N Package



TOP VIEW

CD01244S

A Package



TOP VIEW

CD12570S

8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181, 82S181A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S181 N • N82S181A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S181 A • N82S181A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

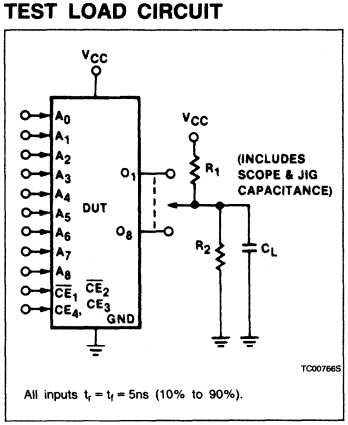
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL} V_{IH} V_{IC}	Low High Clamp	 $I_{IN} = -12mA$	 2.0 	 −0.8	0.8 −1.2	V
Output voltage[2]						
V_{OL} V_{OH}	Low High	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High $I_{OUT} = 9.6mA$ $I_{OUT} = -2mA$	 2.4	 	0.45 	V
Input current[1]						
I_{IL} I_{IH}	Low High	$V_{IN} = 0.45V$ $V_{IN} = 5.5V$	 	 	−100 40	μA
Output current[1]						
I_{OZ} I_{OS}	Hi-Z State Short circuit[3]	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$, $\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$ $\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High stored	 −15	 	40 −40 −70	μA mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$ $V_{OUT} = 2.0V$		5 8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S181			N82S181A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		50	70		45	55	ns
t_{CE}		Output	Chip Enable		25	40		25	40	ns
Disable time[6]										
t_{CD}		Output	Chip disable		25	40		25	40	ns

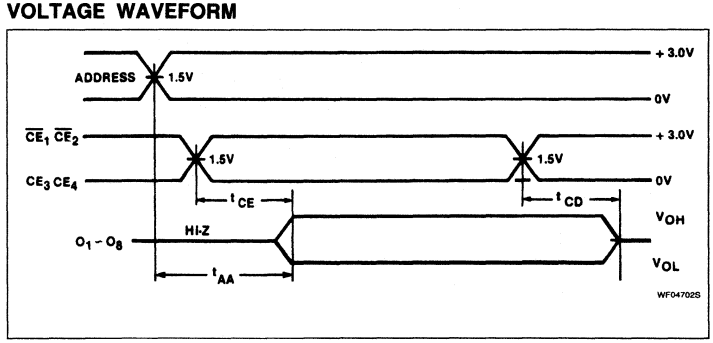
NOTES:
1. Positive current is defined as into the terminal referenced.
1. All voltages with respect to network ground.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORM



Signetics

82S181C
8K-Bit TTL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 82S181C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181C is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

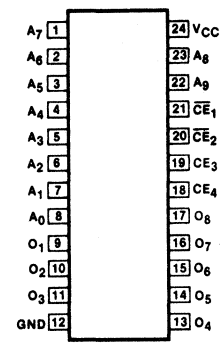
- **Address access time: 35ns max**
- **Power dissipation: 76μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Four Chip Enable inputs**
- **Outputs: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

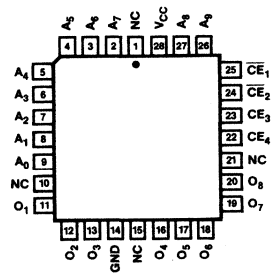
N Package



TOP VIEW

CD01244S

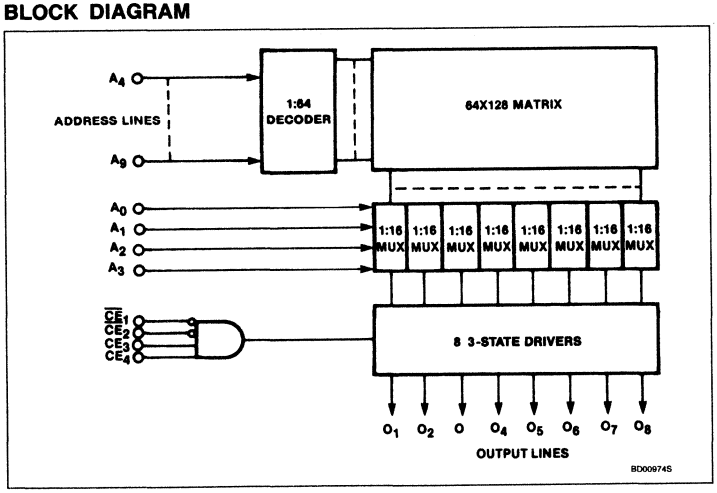
A Package



TOP VIEW

CD12570S

BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S181C N
24-pin Plastic DIP 300mil-wide	N82S181C N3
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S181C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Temperature range Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage[2]						
V_{OL}	Low	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High I_{OUT} = 9.6mA			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

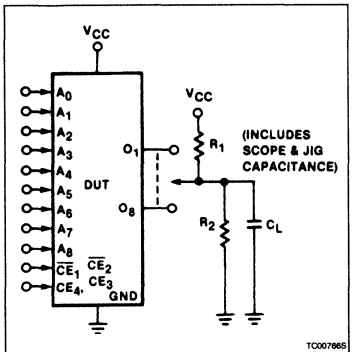
8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181C

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		25	35	ns
t_{CE}		Output	Chip enable		15	20	ns
Disable time[6]							
t_{CD}		Output	Chip disable		15	20	ns

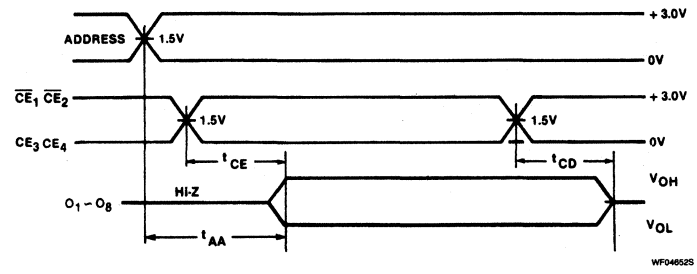
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs: $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORM



All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S183
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S123 is field programmable, which means lowing the that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S183 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the output drivers are controlled solely by $\overline{CE}_1$, $\overline{CE}_2$, and CE_3 lines.

A D-type latch is used to enable the 3-State output drivers. In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of Address or Chip Enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Ordering information can be found on the following page.

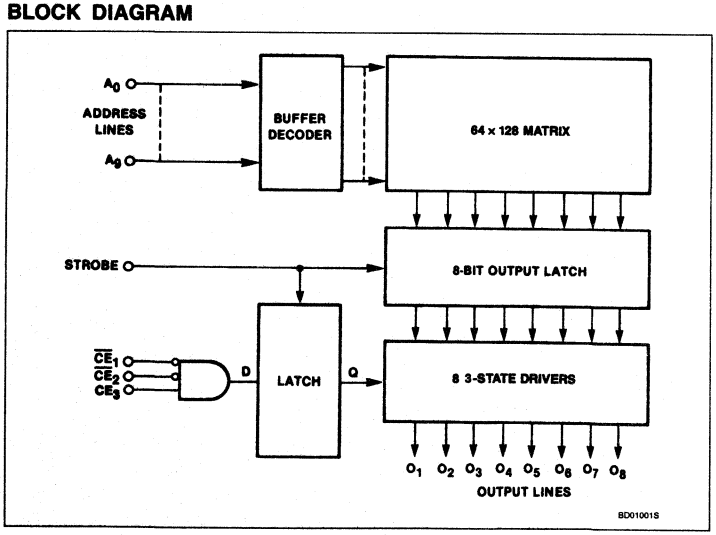
FEATURES

- **Address access time: 60ns max**
- **Power dissipation: 80μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Three Chip Enable inputs**
- **Outputs: 3-State**

APPLICATIONS

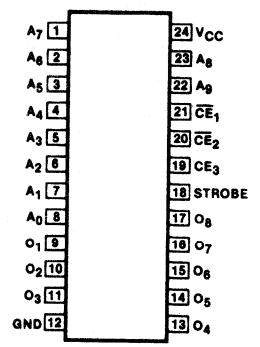
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATIONS

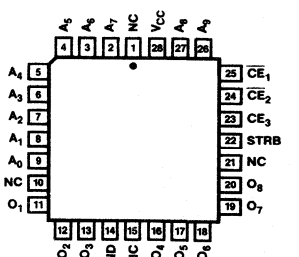
N Package



TOP VIEW

CD01231S

A Package



TOP VIEW

CD12560S

8K-Bit TTL Bipolar PROM (1024 × 8) — 82S183

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S183 N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S183 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

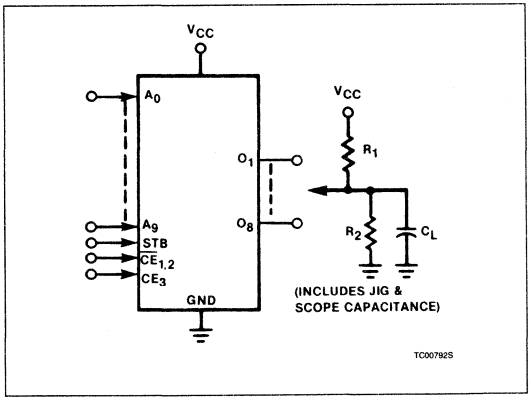
SYMBOL	PARAMETER	TEST CONDITIONS[4]	LIMITS			UNIT
			Min	Typ[6]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}_{1,2}$ = Low, CE_3 = Strobe = High				
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	V
V_{OH}	High	I_{OUT} = −2.0mA	2.4			
Input current[4]						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V	25		25	
Output current[4]						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High or CE = Low, V_{OUT} = 5.5V			40	μA
		$\overline{CE}$ = High or CE = Low, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit[1]	$\overline{CE}$ = Low, CE = High, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[9]						
I_{CC}		V_{CC} = 5.25V		130	175	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High or CE_3 = Low, V_{CC} = 5.0				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

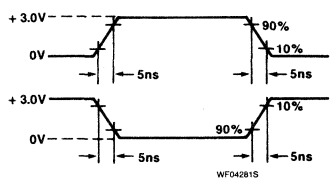
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP[6]	MAX	UNIT
Access time[2]								
t_{AA} t_{CE}		Output Output	Address Chip enable	Latched or transparent read		45 25	60 40	ns
Disable time[2,7]								
t_{CD}		Output	Chip disable	Latched or transparent read		25	40	ns
Setup and hold time[3]								
t_{CDS} t_{CDH}	Setup time Hold time	Output	Chip enable	Latched read only	40 10			ns
t_{ADH}	Hold time	Output	Address		0			
Pulse width[3]								
t_{SW}	Strobe			Latched read only	30	15		ns
Latch time[3]								
t_{SL}	Strobe			Latched read only	60	35		ns
Delatch time[3,7]								
t_{DL}	Strobe			Latched read only			30	ns

NOTES:
1. No more than one output should be grounded at the same time and Strobe should be disabled. Strobe is in High state.
2. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
3. In Latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transfered and chip enable conditions be stored. The new data will appear on the output if the chip enable conditions enable the outputs.
4. Positive current is defined as into the terminal referenced.
5. Areas shown by crosshatch are latched data from previous address.
6. Typical values are $V_{CC} = 5V$, $T_A = +25°C$.
7. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
8. All AC parameters are measured at 1.5V unless otherwise specified.
9. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT

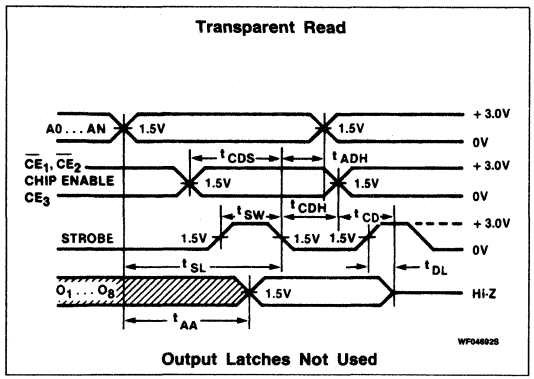


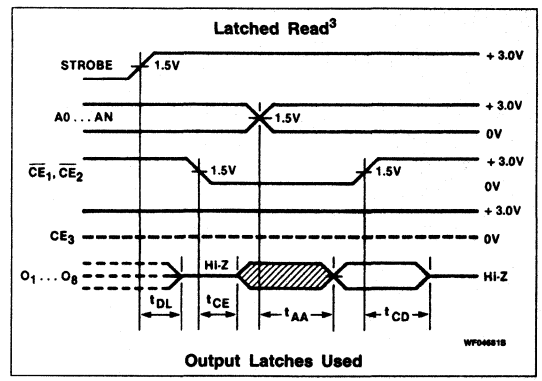
VOLTAGE WAVEFORM



Input Pulses

TIMING DIAGRAMS[8]





Signetics

82S185
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

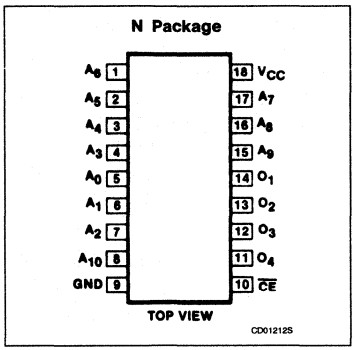
FEATURES

- **Low power dissipation: 50μW/bit typ**
- **Address access time: 100ns max**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Outputs: 3-State**

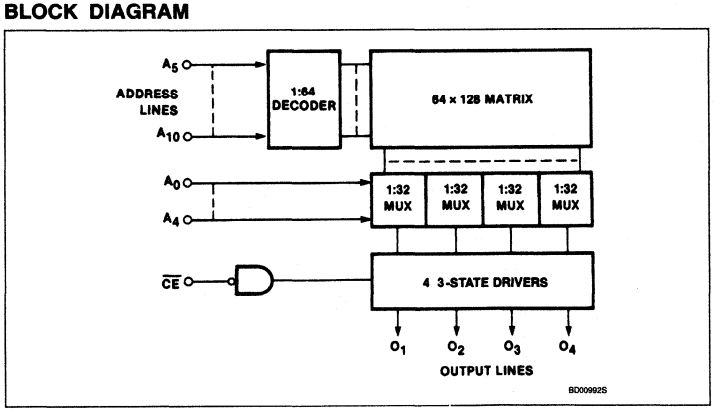
APPLICATIONS

- **Sequential controllers**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (2048 × 4) — 82S185

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S185 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[1]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage[1]						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current[2]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		90	120	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

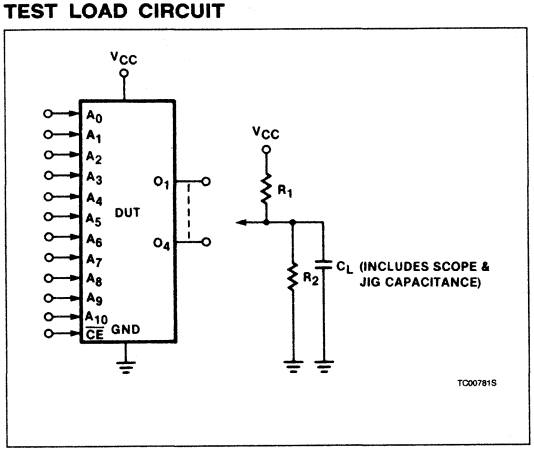
8K-Bit TTL Bipolar PROM (2048 × 4) — 82S185

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

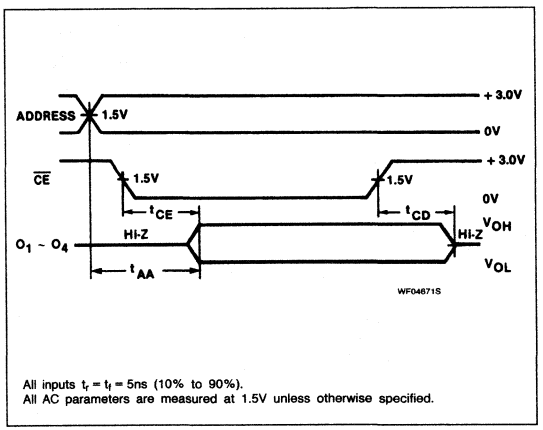
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip Enable		30	40	ns
Disable time[6]							
t_{CD}		Output	Chip disable		30	40	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S185A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185A is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185A device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

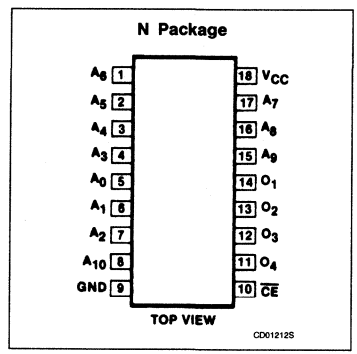
FEATURES

- **Low power dissipation: 70μW/bit typ**
- **Address access time: 50ns max**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Outputs: 3-State**

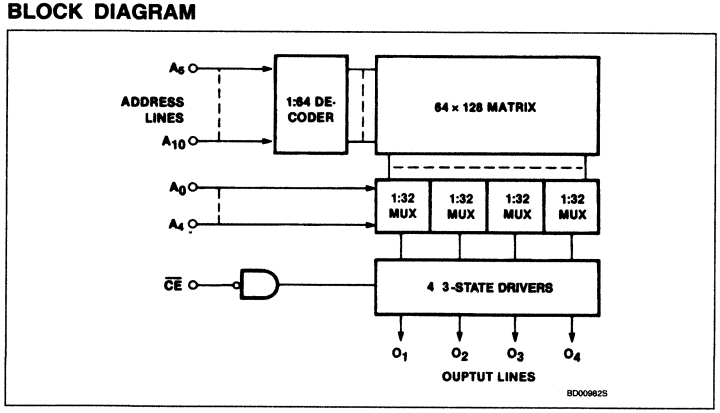
APPLICATIONS

- **Microprogramming**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (2048 × 4) — 82S185A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S185A N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

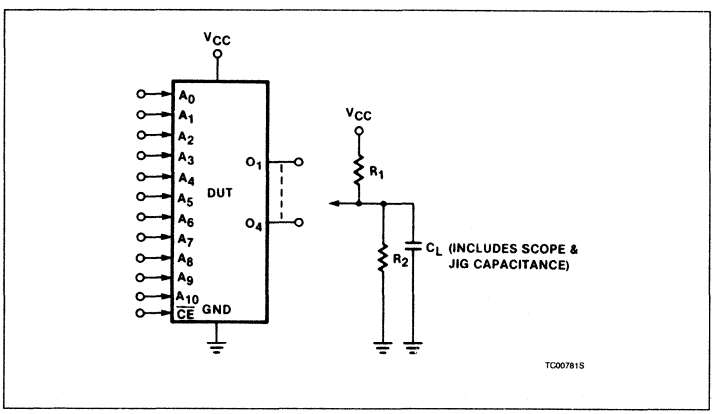
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL} V_{IH} V_{IC}	Low High Clamp	V_{CC} = 4.75V V_{CC} = 5.25V I_{IN} = −12mA	2.0	0.8 −0.8	 −1.2	V
Output voltage						
V_{OL} V_{OH}	Low High	$\overline{CE}$ = Low I_{OUT} = 16mA I_{OUT} = −2mA	 2.4		0.45	V
Input current						
I_{IL} I_{IH}	Low High	V_{IN} = 0.45V V_{IN} = 5.5V			−100 40	μA
Output current						
I_{OZ} I_{OS}	Hi-Z State Short circuit[3]	$\overline{CE}$ = High, V_{OUT} = 0.5V $\overline{CE}$ = High, V_{OUT} = 5.5V $\overline{CE}$ = Low, V_{OUT} = 0V High stored	 −15		−40 40 −70	μA mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		110	155	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	$\overline{CE}$ = High, V_{CC} = 5.0V V_{IN} = 2.0V V_{OUT} = 2.0V		5 8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

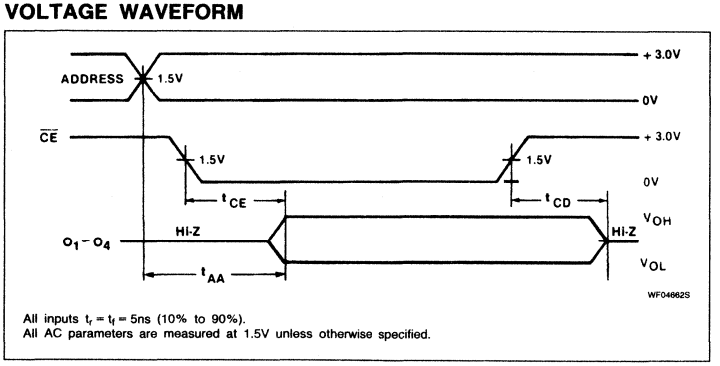
SYMBOL	PARAMETER	TO	FROM	N82S185A			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	50	ns
t_{CE}		Output	Chip Enable		20	30	ns
Disable time[6]							
t_{CD}		Output	Chip disable		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S185C
8K-Bit TTL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 82S185C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185C device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

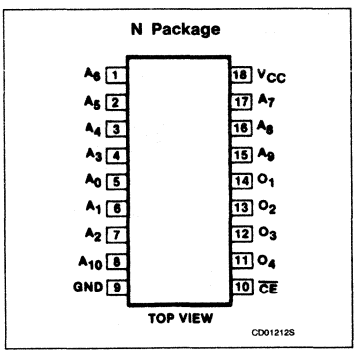
FEATURES

- **Low power dissipation: 70μW/bit typ**
- **Address access time: 25ns max**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Outputs: 3-State**

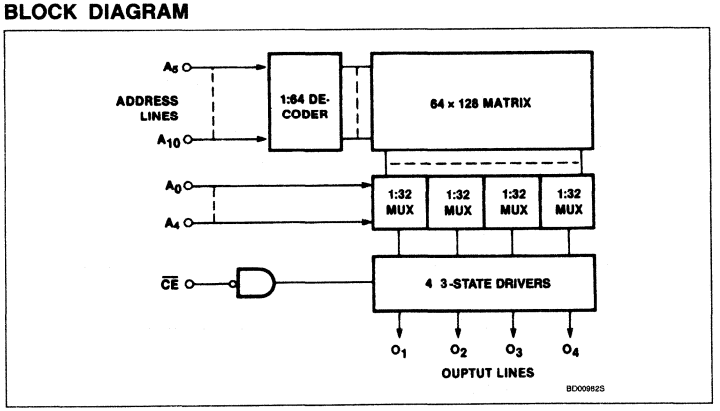
APPLICATIONS

- **Microprogramming**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (2048 × 4) — 82S185C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S185C N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

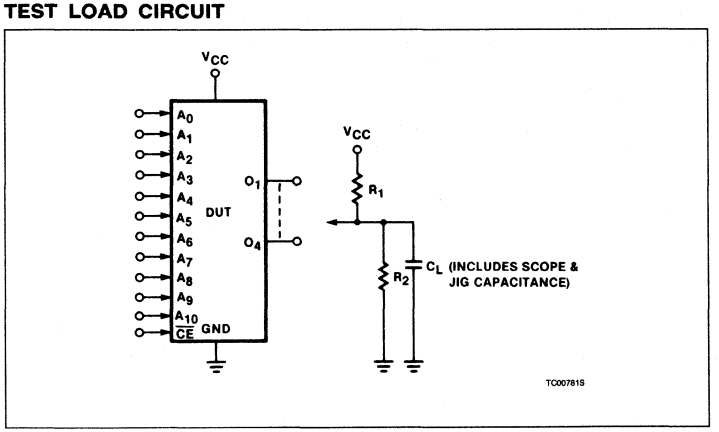
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V		0.8		V
V_{IH}	High	V_{CC} = 5.25V	2.0			
V_{IC}	Clamp	I_{IN} = −12mA		−0.8	−1.2	
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		110	155	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

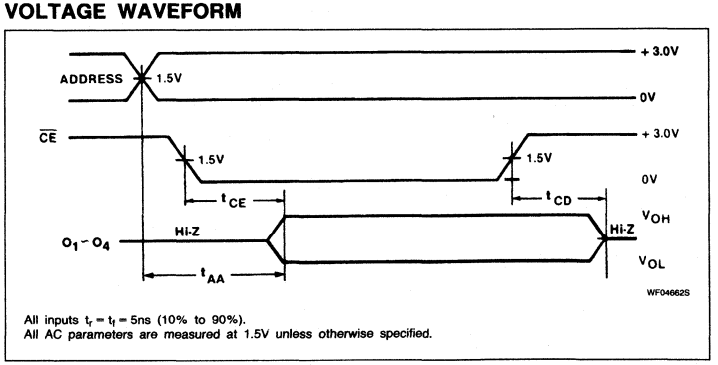
SYMBOL	PARAMETER	TO	FROM	N82S185C			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		20	25	ns
t_{CE}		Output	Chip Enable		10	15	ns
Disable time[6]							
t_{CD}		Output	Chip disable		10	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82HS187
82HS187A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

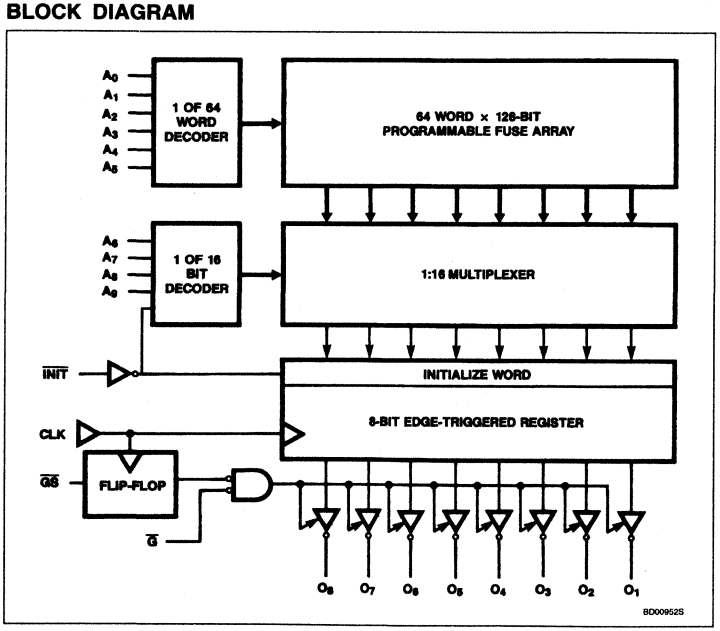
The 82HS187 is a programmable read only memory containing D-type, master-slave data registers. The 82HS187 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is 3-State for ease in connection to bus-organized systems. The combination of on-chip registers and 3-State outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition whenever the Asynchronous Chip Enable ($\overline{G}$) is High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

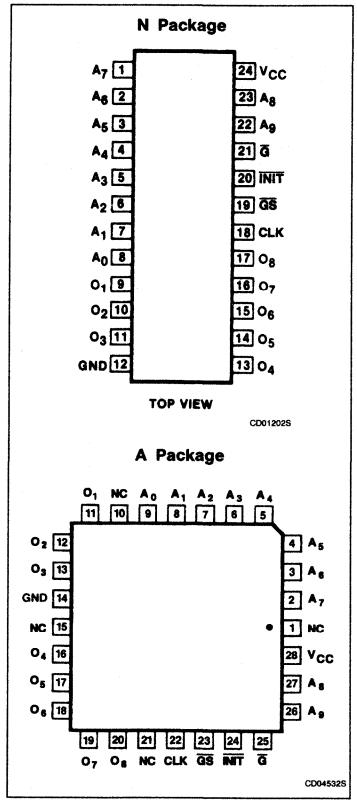
The 82HS187 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the Output Register and will appear at the outputs upon an application of a Low on $\overline{INIT}$ if the outputs are enabled, and will control the state of the data registers independent of all other inputs. The unprogrammed state of $\overline{INIT}$ is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the Addresses and Synchronous Chip Enable can be removed and the output data will remain stable.

BLOCK DIAGRAM



PIN CONFIGURATIONS



FEATURES

- On-chip edge-triggered registers
- Programmable register with Asynchronous initialize function
- 24-pin 300mil-wide DIP package
- Read cycle "Address setup plus clock to output delay"
  - N82HS187: 55ns max
  - N82HS187A: 45ns max
- Outputs: 3-State
- Unprogrammed outputs are High level
- Synchronous and Asynchronous Enables for word expansion

8K-Bit TTL Bipolar PROM (1024 × 8) — 82HS187/82HS187A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	N82HS187 N • N82HS187A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS187 A • N82HS187A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	0°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

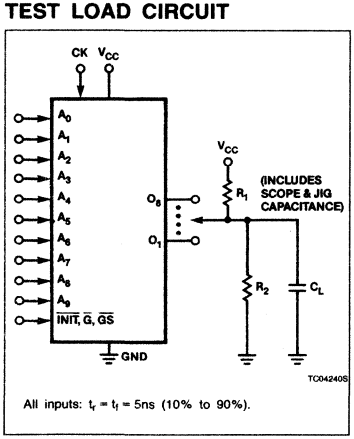
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	
Output voltage[2]						
		$\overline{G}$, $\overline{GS}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{G}$ = High, $V_{OUT} = 5.25V$			40	μA
		$\overline{G}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{G}$, $\overline{GS}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{G}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[4]	TO	FROM	N82HS187			N82HS187A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
t_{CSA} t_{CHA}	Setup Hold	CK	Address	35 0			30 0			ns
t_{OC}	Delay	Output	CK			20	0		15	ns
t_{WC}	Width	H & L	CK	20	10		15	10		ns
t_{CSGS} t_{CHGS}	Setup Hold	CK	$\overline{GS}$	15 5			10 5			ns
t_{OIN}	Delay	Output	$\overline{INIT}$		12	30			25	ns
t_{CIN}	Recovery	CK	$\overline{INIT}$	20	9		15			ns
t_{WIN}	Width		$\overline{INIT}$	25			20			ns
t_{OG}	Delay	Output	$\overline{G}$		11	25			20	ns
t_{OZC}[6]	Delay	Output	CK		16	25			20	ns
t_{OZG}[6]	Delay	Output	$\overline{G}$		14	25			20	ns

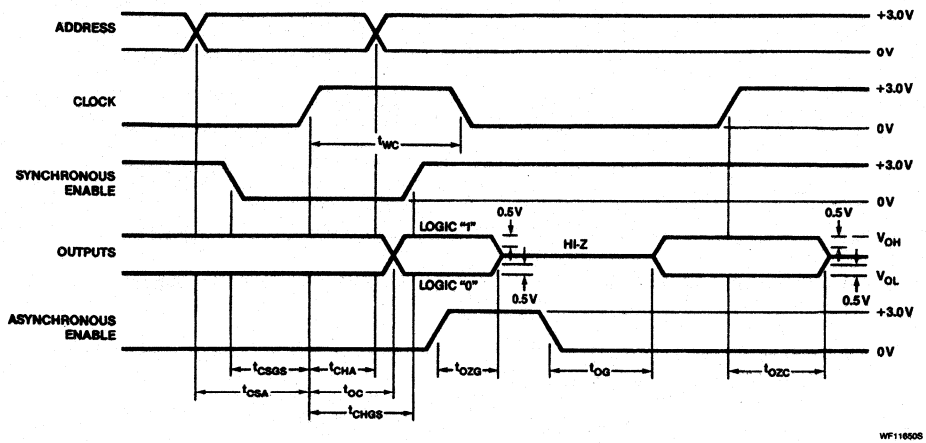
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT

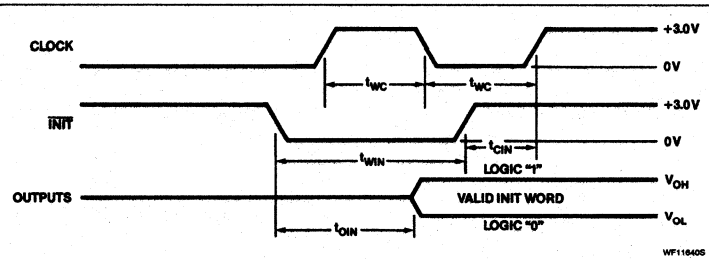


All inputs: $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82HS189
82HS189A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

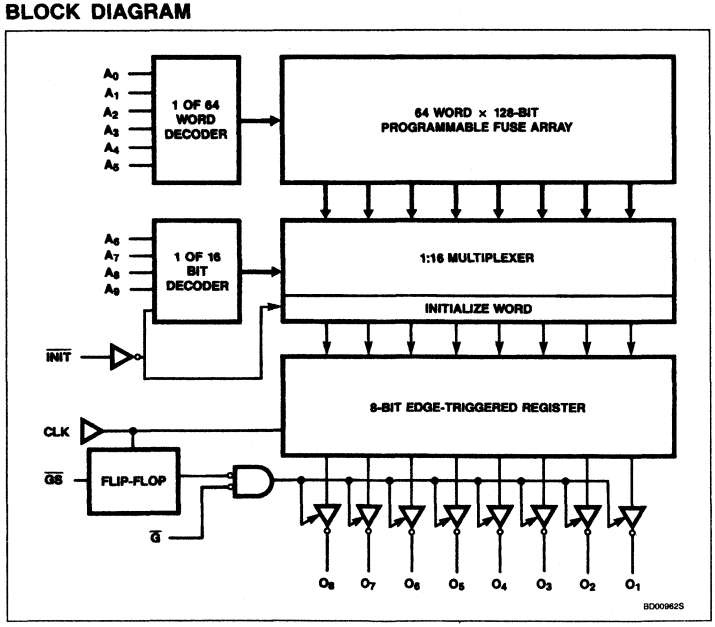
The 82HS189 is a programmable read only memory containing D-type, master-slave data registers. The 82HS189 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is 3-State for ease in connection to bus-organized systems. The combination of on-chip registers and 3-State outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition if the Asynchronous Chip Enable ($\overline{G}$) is held High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

The 82HS189 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the Output Register on the next rising edge of the clock. The unprogrammed state of $\overline{INIT}$ is all ones.

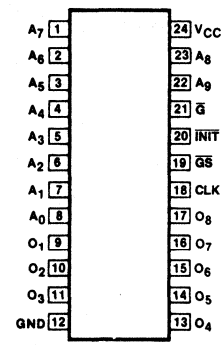
Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the Addresses and Synchronous Chip Enable can be removed and the output data will remain stable.

BLOCK DIAGRAM



PIN CONFIGURATIONS

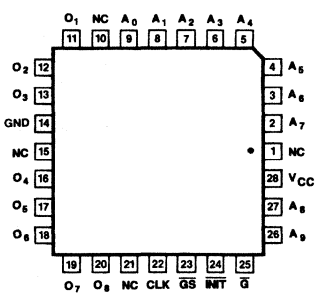
N Package



TOP VIEW

CD01202S

A Package



CD04532S

FEATURES

- On-chip edge-triggered registers
- Asynchronous and Synchronous Enables for word expansion
- Programmable register with synchronous initialize function
- 24-pin 300mil-wide package
- Read cycle "Address setup plus clock to output delay"
  - N82HS189: 55ns max
  - N82HS189A: 45ns max
- Unprogrammed outputs are High level
- Outputs: 3-State

8K-Bit TTL Bipolar PROM (1024 × 8) — 82HS189/82HS189A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	N82HS189 N • N82HS189A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS189 A • N82HS189A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C,\ 4.75V \leqslant V_{CC} \leqslant 5.25V$

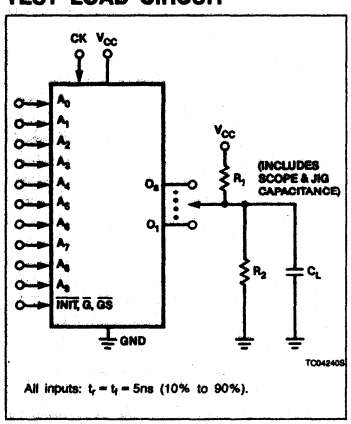
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	
Output voltage[2]						
		$\overline{G}$, $\overline{GS}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{G}$ = High, $V_{OUT} = 5.25V$			40	μA
		$\overline{G}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{G}$, $\overline{GS}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{G}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

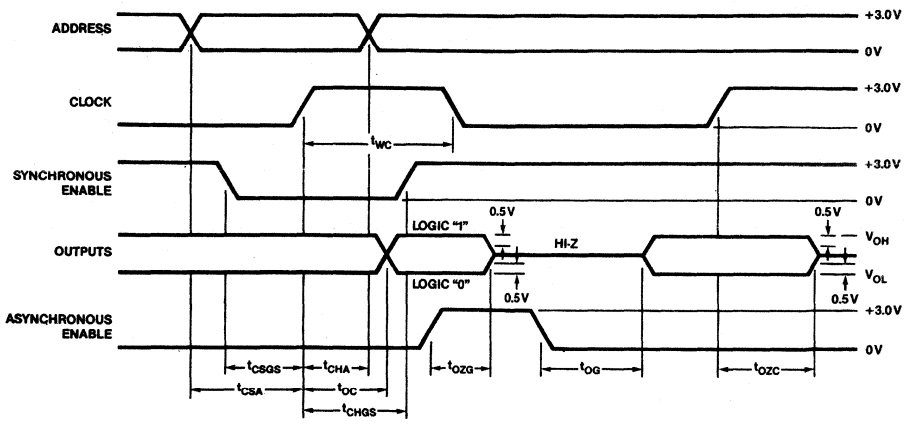
SYMBOL	PARAMETER[4]	TO	FROM	N82HS189			N82HS189A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
t_{CSA} t_{CHA}	Setup Hold	CK	Address	35 0			30 0			ns
t_{OC}	Delay	Output	CK		10	20	0		15	ns
t_{WC}	Width	H & L	CK	20	10		15			ns
t_{CSGS} t_{CHGS}	Setup Hold	CK	$\overline{GS}$	15 5			10 5			ns
t_{CSIN} t_{CHIN}	Setup Hold	CK	$\overline{INIT}$	25 0	8		20 0			ns
t_{OG}	Delay	Output	$\overline{G}$		11	25			20	ns
t_{OZC}[6]	Delay	Output	CK		16	25			20	ns
t_{OZG}[6]	Delay	Output	$\overline{G}$		14	25			20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

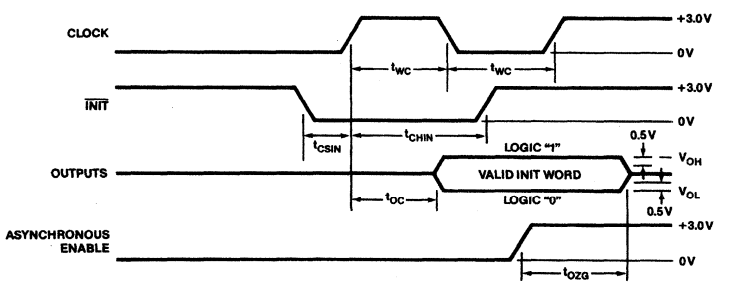
TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

16K-bit TTL Bipolar PROM

Signetics

82S191
82S191A
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S191 and 82S191A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191 and 82S191A are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191 and 82S191A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

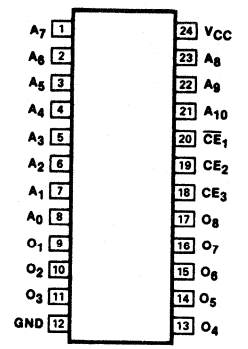
- **Address access time:**
  - **N82S191: 80ns max**
  - **N82S191A: 55ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −100μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

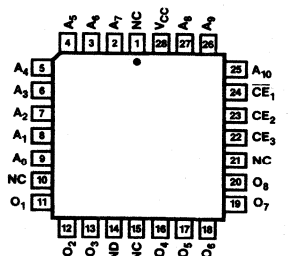
N Package



TOP VIEW

CD01182S

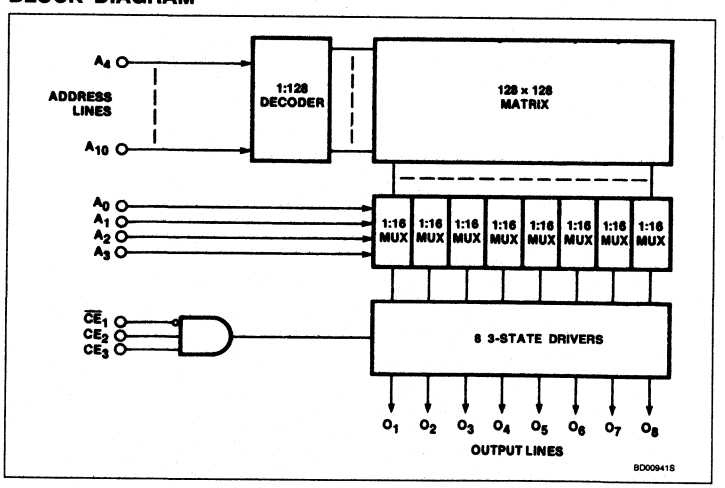
A Package



TOP VIEW

CD12550S

BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S191 N • N82S191A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S191 A • N82S191A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

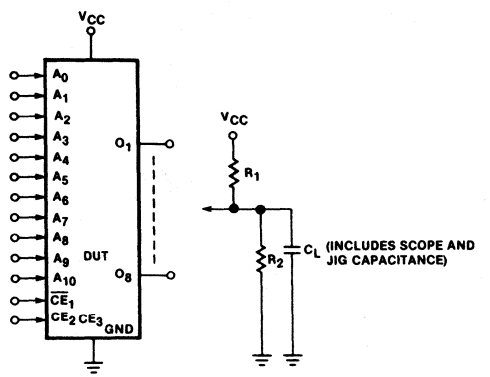
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}_1$ = Low, $CE_{2,3}$ = High				
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			
Input current[1]						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current[1]						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 0.5			−40	μA
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 5.5			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{OUT} = 0V	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

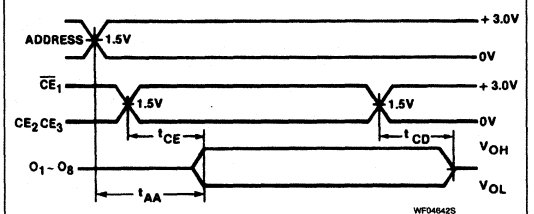
SYMBOL	PARAMETER	TO	FROM	N82S191			N82S191A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
Access time[4]										
t_{AA}		Output	Address		50	80		50	55	ns
t_{CE}		Output	Chip enable		30	40		20	30	ns
Disable time[6]										
t_{CD}		Output	Chip disable		30	40		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82S191C
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S191C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191C is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191C devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

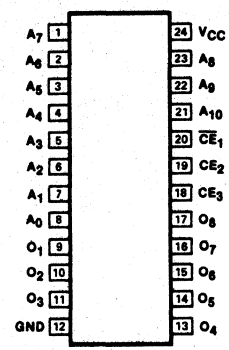
- **Address access time: 35ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −100μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

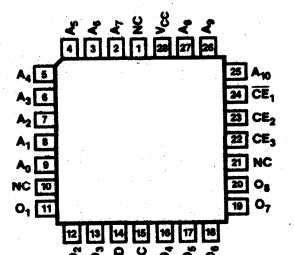
N Package



TOP VIEW

CD011688

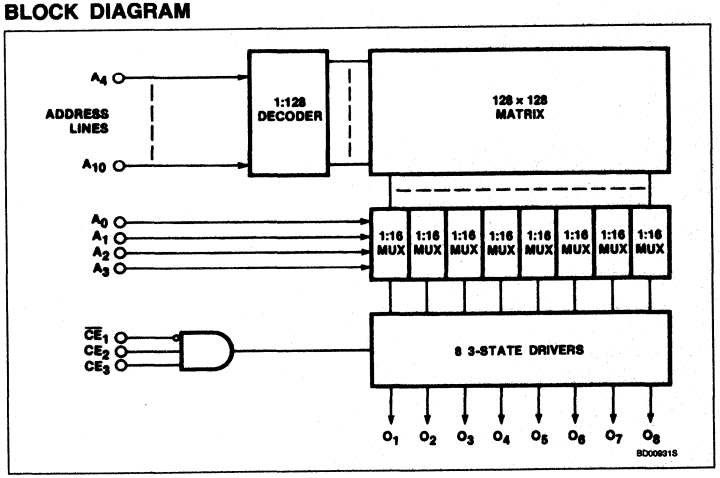
A Package



TOP VIEW

CD12550S

BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (2048 × 8) — 82S191C

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S191C N
24-pin Plastic DIP 300mil-wide	N82S191C N3
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S191C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

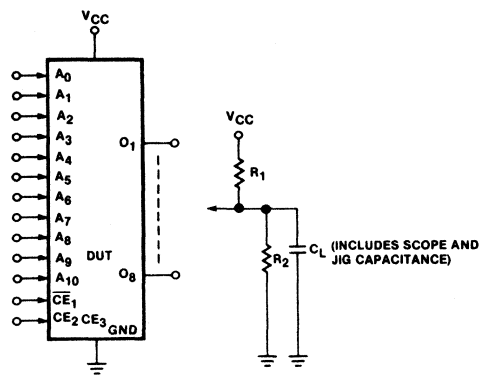
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL} V_{IH} V_{IC}	Low High Clamp	 $I_{IN} = -12mA$	 2.0 	 −0.8	0.8 −1.2	V
Output voltage						
V_{OL} V_{OH}	Low High	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High $I_{OUT} = 9.6mA$ $I_{OUT} = -2mA$	 2.4		0.45	V
Input current						
I_{IL} I_{IH}	Low High	$V_{IN} = 0.45V$ $V_{IN} = 5.5V$			−100 40	μA
Output current						
I_{OZ} I_{OS}	Hi-Z state Short circuit[3]	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 0.5$ $\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 5.5$ $\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $V_{OUT} = 0V$	 −15	 	−40 40 −70	μA mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
C_{IN} C_{OUT}	Input Output	$V_{CC} = 5.0V$ $V_{IN} = 2.0V$ $V_{OUT} = 2.0V$		5 8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

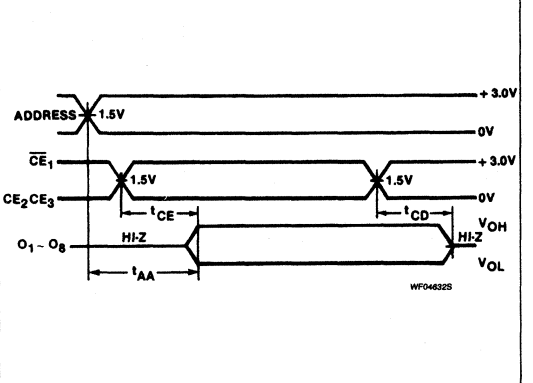
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		30	35	ns
t_{CE}		Output	Chip enable		15	20	ns
Disable time[6]							
t_{CD}		Output	Chip disable		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82HS191
16K-Bit TTL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 82HS191 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82HS191 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82HS191 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

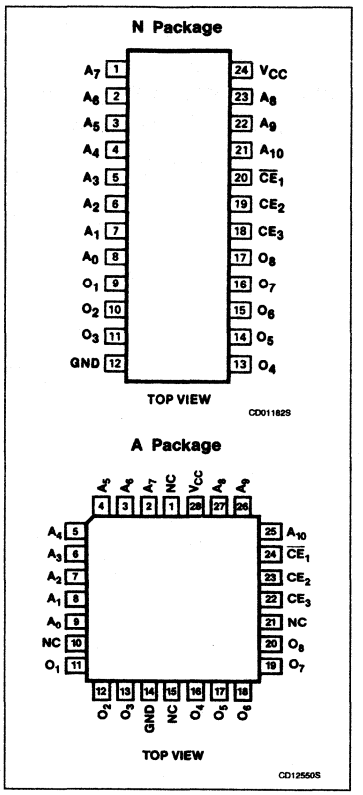
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −250μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: 3-State**

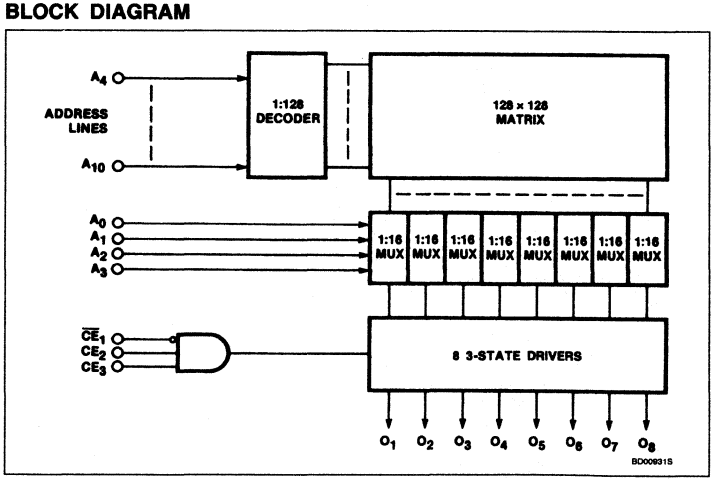
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (2048 × 8) — 82HS191

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82HS191 N
24-pin Plastic DIP 300mil-wide	N82HS191 N3
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS191 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Temperature range Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[5]	LIMITS Max	UNIT
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, I_{OUT} = 16mA			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 5.25$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

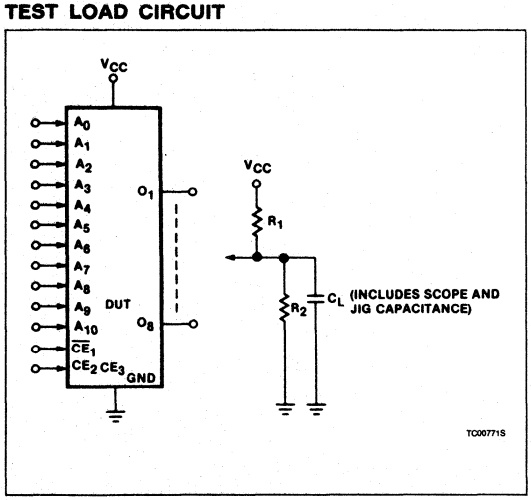
16K-Bit TTL Bipolar PROM (2048 × 8) — 82HS191

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

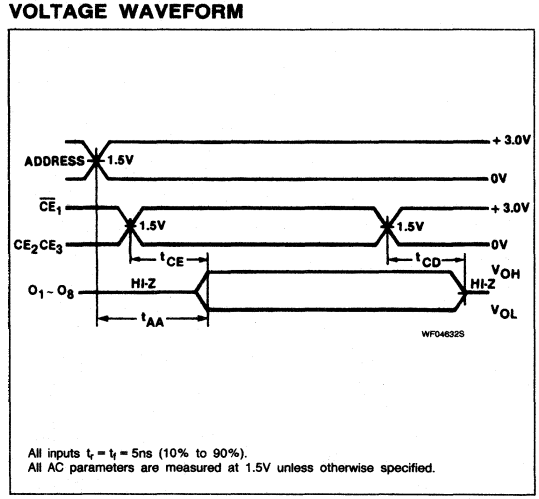
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		15	20	ns
t_{CE}		Output	Chip enable		10	15	ns
Disable time[6]							
t_{CD}		Output	Chip disable		10	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Signetics

82HS195
82HS195A
82HS195B
16K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS195 is field programmable, which means that custom patterns are immediately available by following the Generic II fusing procedure. The Signetics 82HS195 is supplied with all outputs at logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 Chip Enable inputs for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

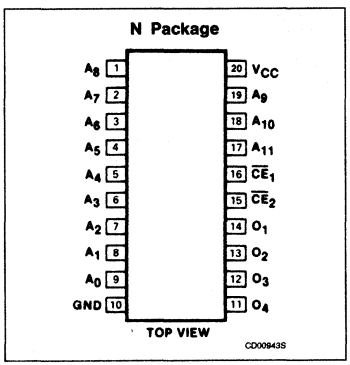
Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

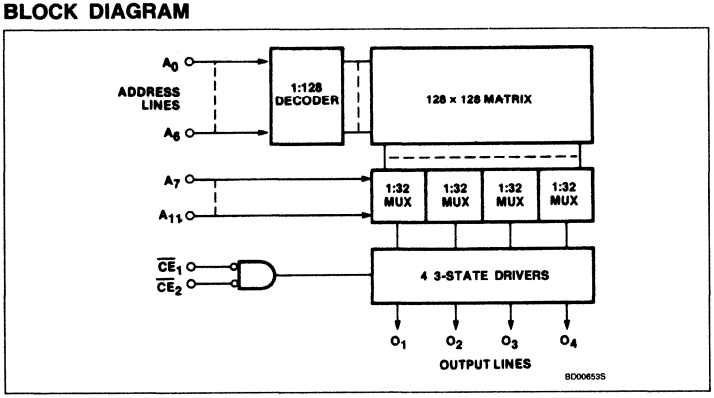
FEATURES

- **Low power dissipation: 35μW/bit typ**
- **Address access time:**
  - **N82HS195: 45ns max**
  - **N82HS195A: 35ns max**
  - **N82HS195B: 25ns max**
- **Input loading: −250μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82HS195 N • N82HS195A N • N82HS195B N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
	Temperature range		
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

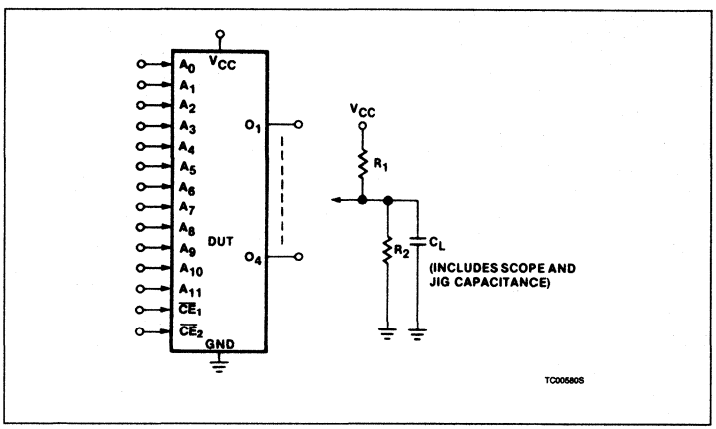
SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}_1$ & $\overline{CE}_2$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{OUT} = 5.25V$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ & $\overline{CE}_2$ = Low, $V_{OUT} = 0V$, High stored	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		120	145	mA
Capacitance						
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

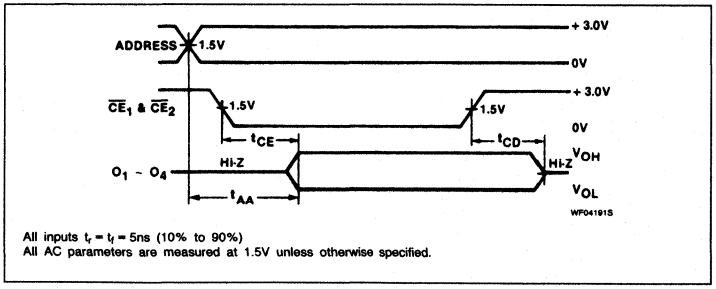
SYMBOL	PARAMETER	TO	FROM	N82HS195			N82HS195A			N82HS195B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[7]													
t_{AA}		Output	Address		35	45		25	35		20	25	ns
t_{CE}		Output	Chip Enable		20	25		15	20		10	15	ns
Disable time[6]													
t_{CD}		Output	Chip disable		20	25		15	20		10	15	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of the short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

32K-bit TTL Bipolar PROM

Signetics

82HS321
82HS321A
82HS321B
32K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

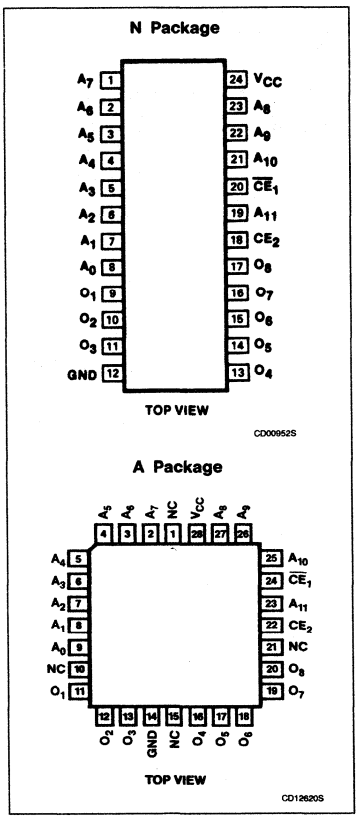
FEATURES

- **Address access time:**
  N82HS321: 45ns max
  N82HS321A: 35ns max
  N82HS321B 30ns max
- **Power dissipation: 20μW/bit typ**
- **Input loading: −250μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

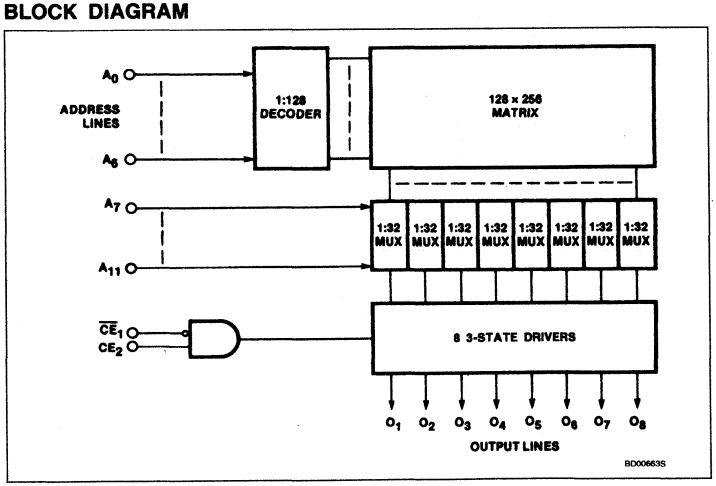
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82HS321 N • N82HS321A N • N82HS321B N
24-pin Ceramic DIP 600mil-wide	N82HS321 F • N82HS321A F • N82HS321B F
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS321 A • N82HS321A A • N82HS321B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

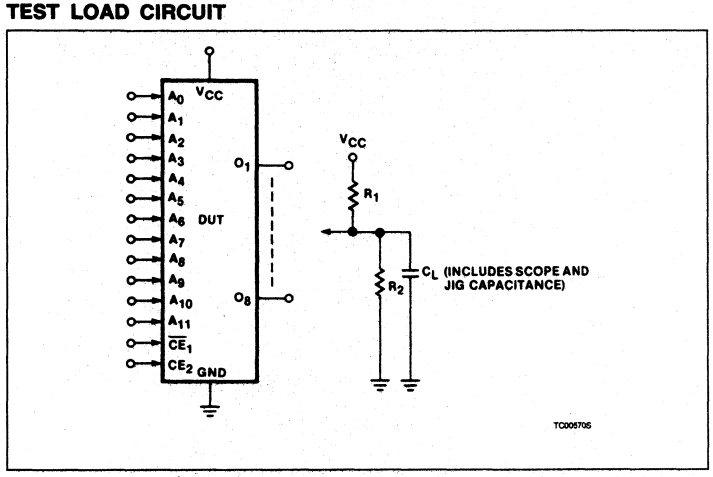
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low, CE_2 = High I_{OUT} = 16mA			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 5.25$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_1$ = High, CE_2 = Low, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

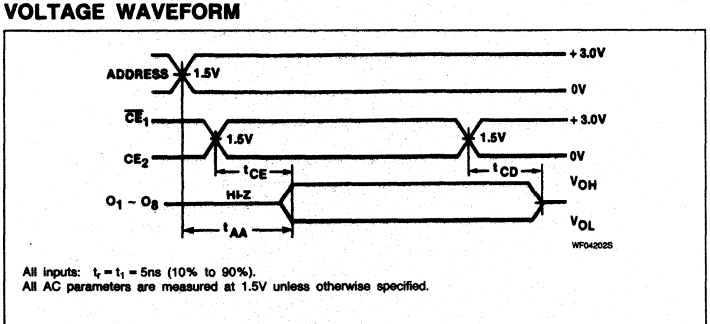
SYMBOL	PARAMETER	TO	FROM	N82HS321			N82HS321A			N82HS321B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[7]													
t_{AA}		Output	Address		40	45		30	35		25	30	ns
t_{CE}		Output	Chip enable		25	30		20	25		18	20	ns
Disable time[6]													
t_{CD}		Output	Chip disable		25	30		20	25		18	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

64K-bit TTL Bipolar PROM

Signetics

82HS641
82HS641A
82HS641B
64K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

The 82HS641 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 Chip Enable input for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

This device is also processed to military requirements for operating over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

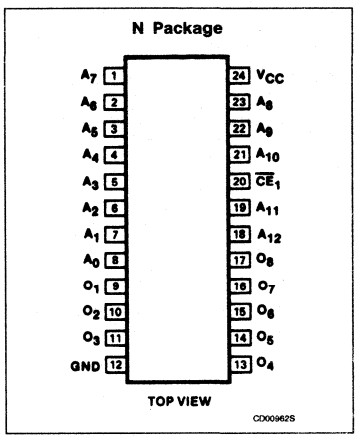
FEATURES

- **Address access time:**
  - **N82HS641 55ns max**
  - **N82HS641A 45ns max**
  - **N82HS641B 35ns max**
- **Power dissipation: 10μW/bit typ**
- **Input loading: −250μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

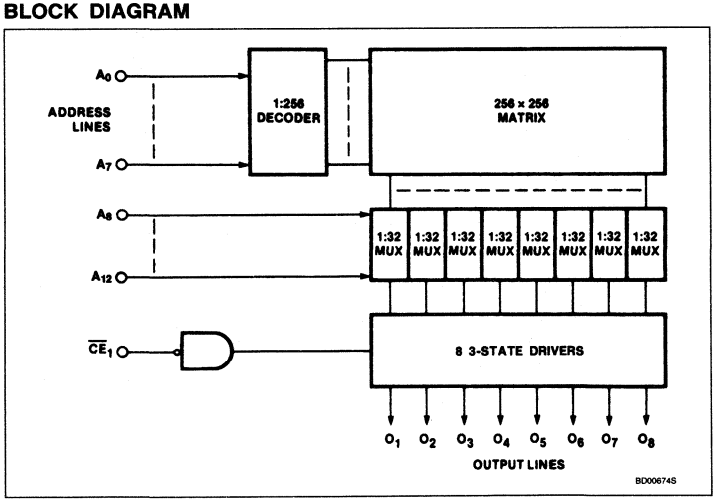
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



64K-Bit TTL Bipolar PROM (8192 × 8) — 82HS641, 82HS641A, 82HS641B

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82HS641 N • N82HS641A N • N82HS641B N
24-pin Ceramic DIP 600mil-wide	N82HS641 F • N82HS641A F • N82HS641B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

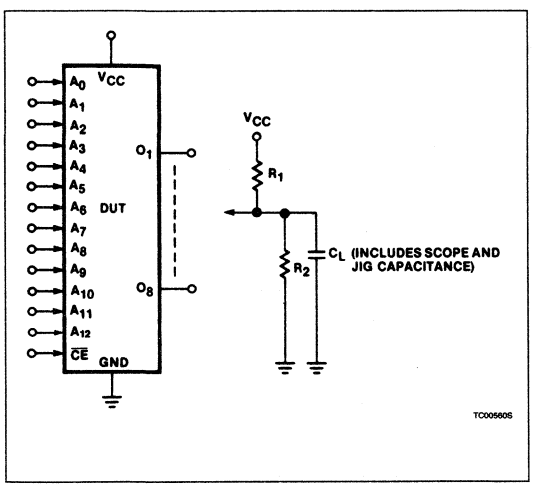
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low $I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$ = High, $V_{OUT} = 5.25V$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_1$ = High $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

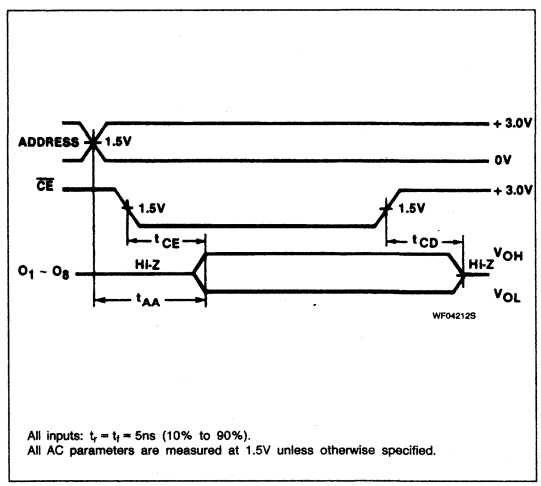
SYMBOL	PARAMETER	TO	FROM	N82HS641			N82HS641A			N82HS641B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[7]													
t_{AA}		Output	Address		50	55		40	45		30	35	ns
t_{CE}		Output	Chip Enable		30	35		20	25		15	20	ns
Disable time[6]													
t_{CD}		Output	Chip disable		30	35		20	25		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

128K-bit TTL Bipolar Prom

Signetics

82HS1281
128K-Bit TTL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 82HS1281 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS1281 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

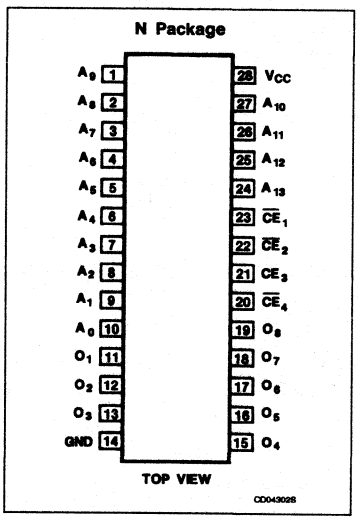
FEATURES

- **Address access time: 45ns max**
- **Power dissipation: 5μW/bit typ**
- **Input loading: −250μA max**
- **Four Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are high level**
- **Fully TTL compatible**
- **Outputs: 3-State**

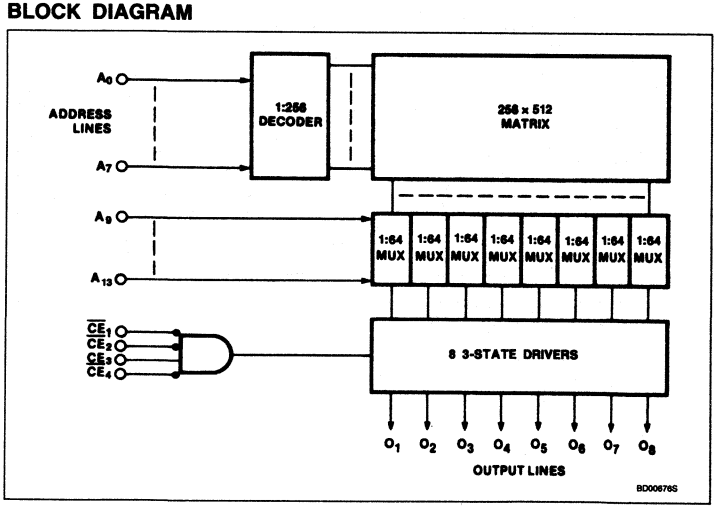
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



128K-Bit TTL Bipolar PROM (16384 × 8) — 82HS1281

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	N82HS1281 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	
Output voltage						
		$\overline{CE}_3$ = High, $\overline{CE}_{1,2,4}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	
Output current						
I_{OZ}	Hi-Z State	CE_3 = Low, $\overline{CE}_{1,2,4}$ = High, $V_{OUT} = 0.5V$			−40	
		CE_3 = Low, $\overline{CE}_{1,2,4}$ = High, $V_{OUT} = 5.25V$			40	
I_{OS}	Short circuit[4]	CE_3 = High, $\overline{CE}_{1,2,4}$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		130	185	mA
Capacitance						
		CE_3 = High, $\overline{CE}_{1,2,4}$ = Low $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

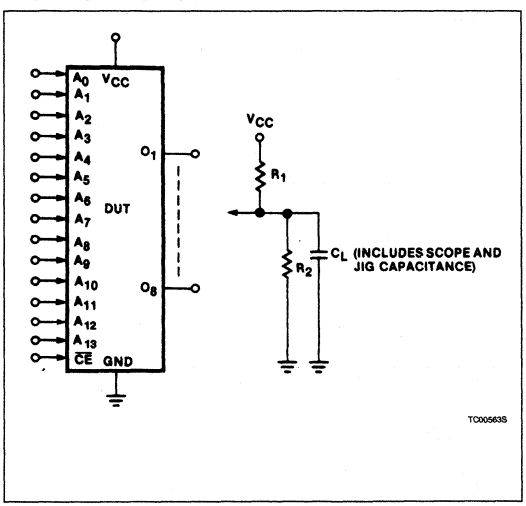
128K-Bit TTL Bipolar PROM (16384 × 8) — 82HS1281

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

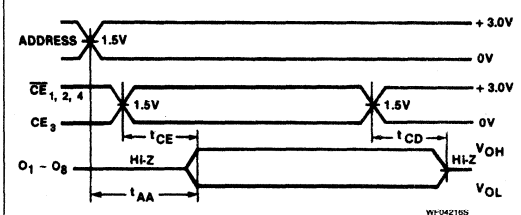
SYMBOL	PARAMETER	TO	FROM	N82HS1281			UNIT
				Min	Typ[5]	Max	
Access time[7]							
t_{AA}		Output	Address			45	ns
t_{CE}		Output	Chip enable			25	ns
Disable time[6]							
t_{CD}		Output	Chip disable			25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of the short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

ECL MEMORIES

Bipolar ECL RAM

Signetics

10422B
1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10422B device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratchpad, control, and buffer storage applications. The 10422B is available in a slimline 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to V_{CC} is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

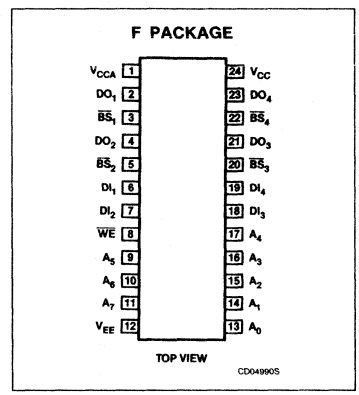
FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 10K series ECL families**
- **Address access time:**
  - 10422B, 10ns max.
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +75°C (ambient)**
- **Block select allows variable organization**

APPLICATIONS

- **High-speed scratchpad**
- **Control and buffer storage**

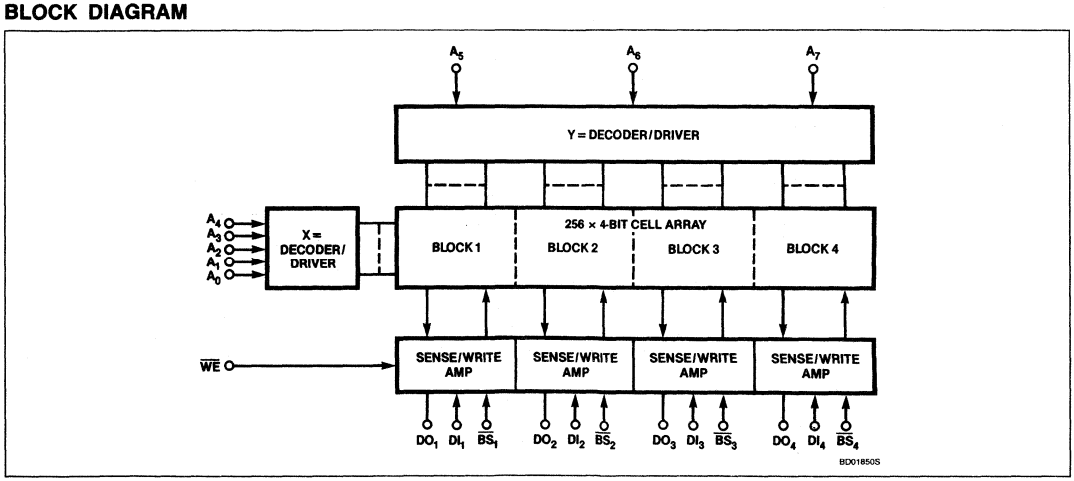
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	+0.5 to −7	V_{DC}
V_{IN}	Input voltage	0 to V_{EE}	
I_O	Output current	−30	mA
T_A	Operating ambient temperature	0 to +75	°C
T_J	Operating junction temperature	+125	
T_{STG}	Storage temperature	−55 to +150	

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4) — 10422B

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual-In-line 400mil wide 24-pin	10422B F

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

PARAMETER		TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
			Min	Max	Min	Max	Min	Max	
Input voltage									
V_{IH}	High		−1.145	−0.840	−1.105	−0.810	−1.045	−0.720	V
V_{IL}	Low		−1.870	−1.490	−1.850	−1.475	−1.830	−1.450	
Output voltage									
V_{OH}	High	V_{IH} = Max	−1.0	−0.840	−0.960	−0.810	−0.900	−0.720	
V_{OL}	Low	V_{IL} = Min	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	V
V_{OHT}	Threshold HIGH	V_{IH} = Min	−1.020		−0.980		−0.920		
V_{OLT}	Threshold LOW	V_{IL} = Max		−1.645		−1.630		−1.605	
Input current									
I_{IH}	High	V_{IH} = Max		220		220		220	μA
I_{IL}	Low	V_{IL} = Min	−50		−50		−50		
I_{IL}	$\overline{BS}$	V_{IL} = Min	0.5		0.5		0.5		
I_{EE}	Supply current	V_{IL} = Min		200		200		200	mA

NOTES:
1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $+75°C$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{AA}	Address access time			10	ns
t_{RBS}	Block select recovery time			5	
t_{ABS}	Block select access time			5	
t_{WD}	Write disable time			5	
t_{WPW}	Write pulse width	7			
t_{WR}	Write recovery time		4.5	9	
t_{WHA}	Address hold time	2	1		
t_{WHBS}	Block select hold time	2	1		
t_{WHD}	Data hold time	2	1		
t_{WSA}	Address setup time	3	1		
t_{WSBS}	Block select setup time	2	1		
t_{WSD}	Data setup time	2	1		
t_f	Output fall time		2		
t_r	Output rise time		2		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

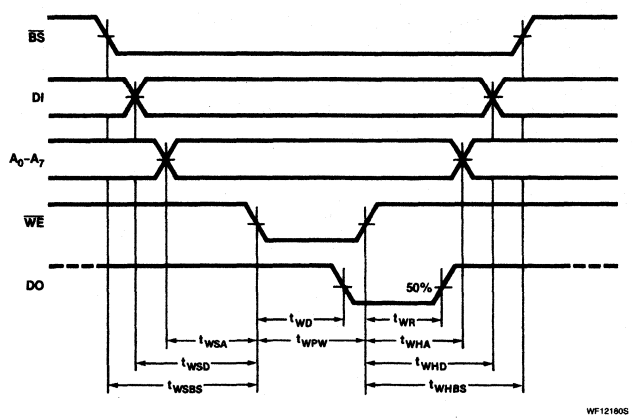
NOTES:
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

TRUTH TABLE

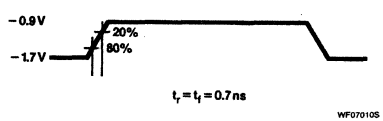
MODE	INPUTS			OUTPUTS
	$\overline{BS}_N$	$\overline{WE}$	DI_N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't Care
N = Blocks 1 – 4

TIMING DIAGRAMS

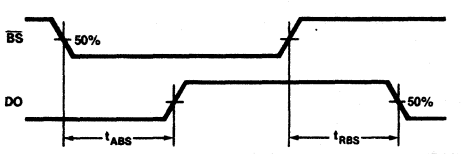


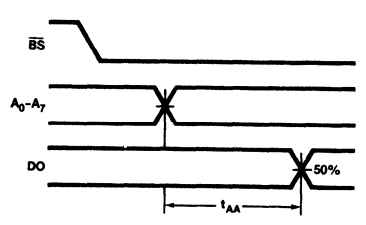
Write Mode



NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels





Read Mode

Signetics

10422C
1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10422C device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratch pad, control, and buffer storage applications. The 10422C is available in a slimline 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to V_{CC} is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

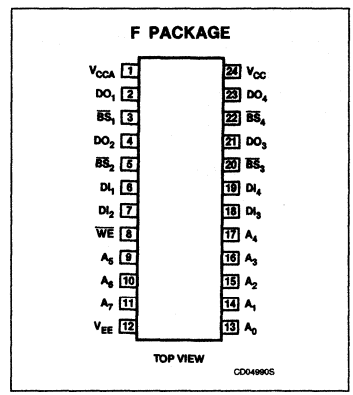
FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 10K series ECL families**
- **Address access time:**
  - **10422C, 7ns max**
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +75°C (ambient)**
- **Block select allows variable organization**

APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

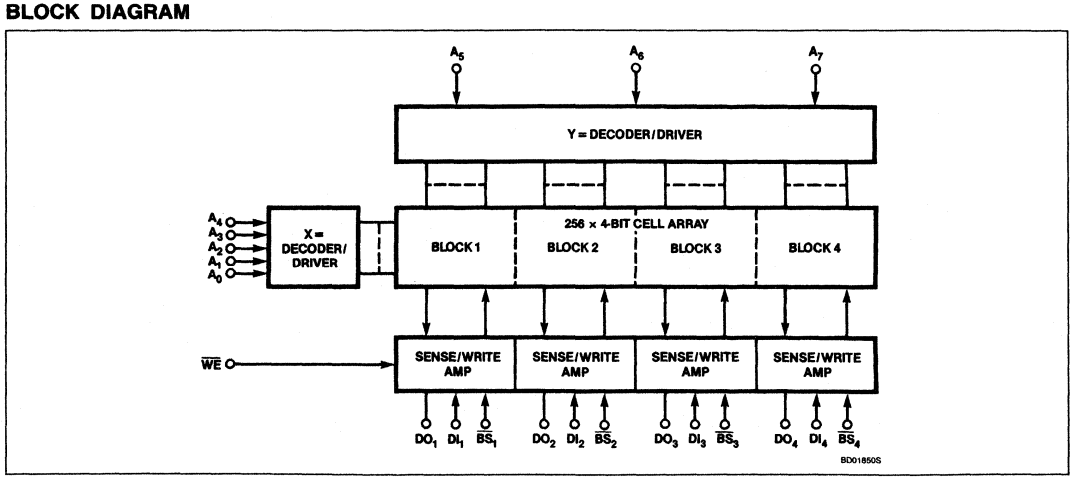
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	+0.5 to −7	V_{dc}
V_{IN}	Input voltage	0 to V_{EE}	V_{dc}
I_O	Output current	−30	mA
T_A	Operating	0 to +75	°C
T_J	Operating junction	125	°C
T_{STG}	Storage	−55 to +150	°C

BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 400mil wide 24-pin	10422C F

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

PARAMETER		TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
			Min	Max	Min	Max	Min	Max	
Input voltage									
V_{IH}	High		−1.145	−0.840	−1.105	−0.810	−1.045	−0.720	V
V_{IL}	Low		−1.870	−1.490	−1.850	−1.475	−1.830	−1.450	
Output voltage									
V_{OH}	High	V_{IH} = Max	−1.0	−0.840	−0.960	−0.810	−0.900	−0.720	
V_{OL}	Low	V_{IL} = Min	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	V
V_{OHT}	Threshold HIGH	V_{IH} = Min	−1.020		−0.980		−0.920		
V_{OLT}	Threshold LOW	V_{IL} = Max		−1.645		−1.630		−1.605	
Input current									
I_{IH}	High	V_{IH} = Max		220		220		220	μA
I_{IL}	Low	V_{IL} = Min	−50		−50		−50		
I_{IL}	$\overline{BS}$	V_{IL} = Min	0.5		0.5		0.5		
I_{EE}	Supply current	V_{IL} = Min		200		200		200	mA

NOTES:
1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $+75°C$

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{AA}	Address access time			7	ns
T_{RBS}	Block select recovery time		4		
T_{ABS}	Block select access time		6		
T_{WD}	Write disable time		4		
T_{WPW}	Write pulse width	5			
T_{WR}	Write recovery time		6		
T_{WHA}	Address hold time		1		
T_{WHBS}	Block select hold time		1		
T_{WHD}	Data hold time		1		
T_{WSA}	Address setup time		1		
T_{WSBS}	Block select setup time		1		
T_{WSD}	Data setup time		1		
t_f	Output fall time		2		
t_r	Output rise time		2		
Capacitance					
C_{IN}	Input			8	pF
C_{OUT}	Output			8	

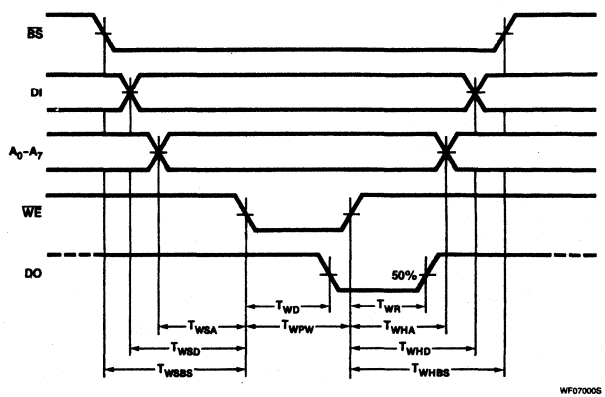
NOTES:
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

TRUTH TABLE

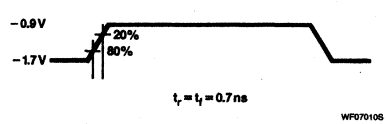
MODE	INPUTS			OUTPUTS
	$\overline{BS}_N$	$\overline{WE}$	DI_N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
N = Blocks 1 – 4

TIMING DIAGRAMS

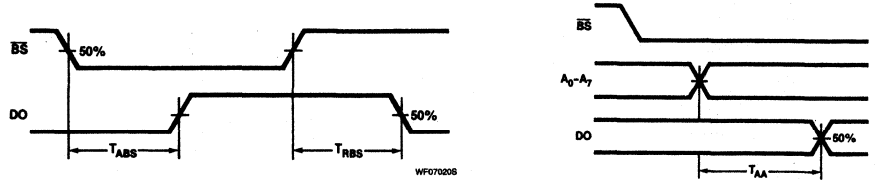


Write Mode



NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels



Read Mode

Signetics

100422B
1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100422B device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratchpad, control, and buffer storage applications. The 100422B contains voltage and temperature compensation circuits making it 100K family compatible. The 100422B is available in a slimline 24-pin dual-in-line package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply voltage. The input pull-down resistor to V_{EE} is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

FEATURES

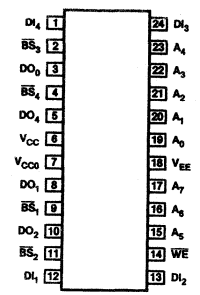
- **256 words × 4 bits organization**
- **Fully compatible with 100K series ECL families**
- **Address access time:**
  - 100422B: 10ns max.
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +85°C**
- **Block select allows variable organization**

APPLICATIONS

- **High-speed scratchpad**
- **Control and buffer storage**

PIN CONFIGURATION

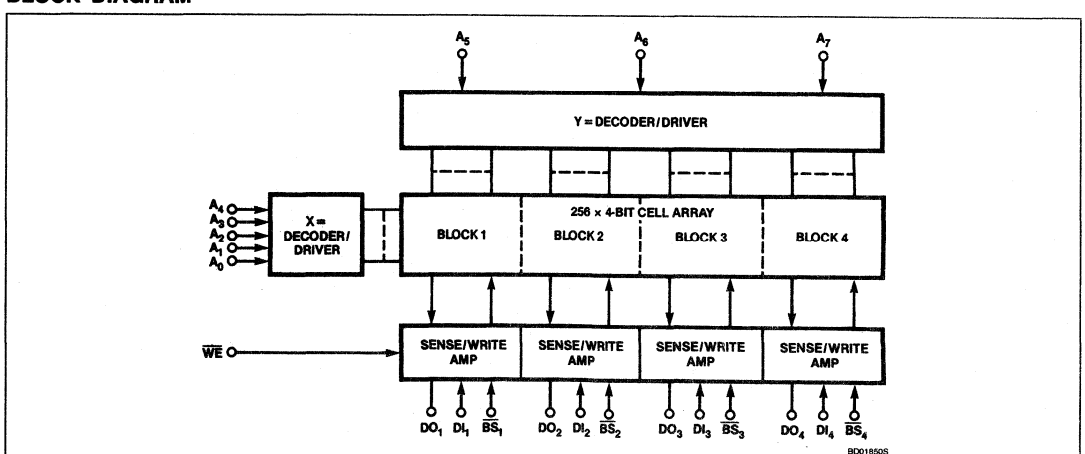
F PACKAGE



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	+0.5 to −7	V_{DC}
V_{IN}	Input voltage	0 to V_{EE}	V_{DC}
I_O	Output current	−30	mA
T_A	Operating ambient temperature	0 to +85	°C
T_J	Operating junction temperature	+125	°C
T_{STG}	Storage temperature	−55 to +150	°C

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4) 100422B

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual-In-line 400mil wide 24-pin	100422B F

DC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V± 5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low		−1.810		−1.475	V
V_{IH}	High		−1.165		−0.880	
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810	−1.715	−1.620	V
V_{OH}	High	V_{IH} = Max	−1.025	−0.955	−0.880	
V_{OLT}	Threshold LOW	V_{IL} = Max			−1.610	
V_{OHT}	Threshold HIGH	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	−50			μA
I_{IL}	$\overline{BS}$	V_{IL} = Min	+0.5			
I_{IH}	High	V_{IH} = Max			220	
I_{EE}	Supply current				210	mA

NOTES:
1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V± 5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{AA}	Address access time			10	ns
t_{RBS}	Block select recovery time			5	
t_{ABS}	Block select access time			5	
t_{WD}	Write disable time			5	
t_{WPW}	Write pulse width	7			
t_{WR}	Write recovery time		4.5	9	
t_{WHA}	Address hold time	2	1		
t_{WHBS}	Block select hold time	2	1		
t_{WHD}	Data hold time	2	1		
t_{WSA}	Address setup time	3	1		
t_{WSBS}	Block select setup time	2	1		
t_{WSD}	Data setup time	2	1		
t_f	Output fall time		2		
t_r	Output rise time		2		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

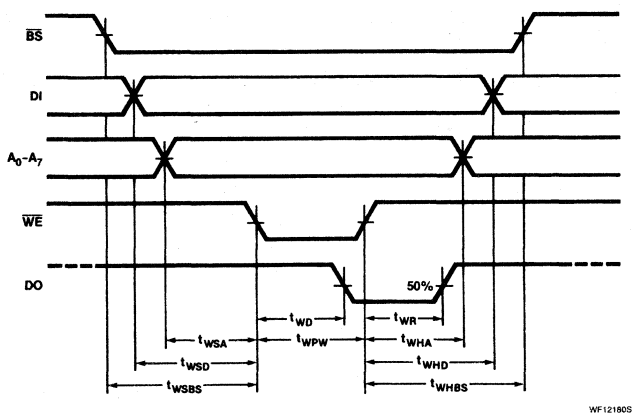
NOTES:
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

TRUTH TABLE

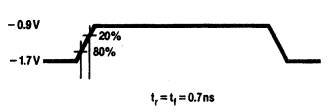
MODE	INPUTS			OUTPUTS
	$\overline{BS_N}$	$\overline{WE}$	DI_N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't Care
N = Blocks 1 – 4

TIMING DIAGRAMS

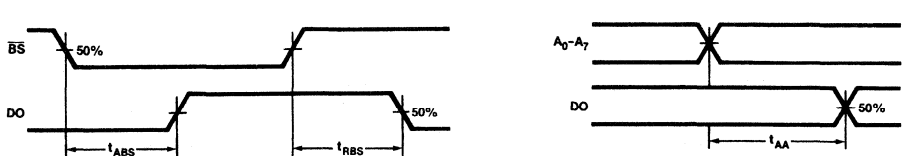


Write Mode



NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels



Read Mode

Signetics

100422C
1K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100422C device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratch pad, control, and buffer storage applications. The 100422C contains voltage and temperature compensation circuits making it 100K family compatible. The 100422C is available in a slimline 24-pin dual-in-line package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply voltage. The input pull-down resistor to V_{EE} is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

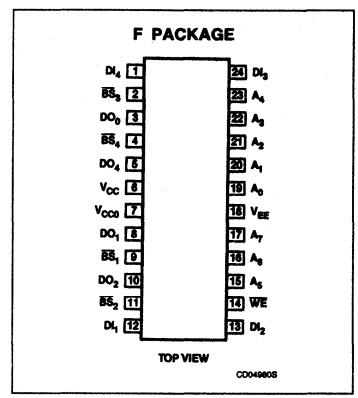
FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 100K series ECL families**
- **Address access time:**
  - **100422C: 7ns max**
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +85°C**
- **Block select allows variable organization**

APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

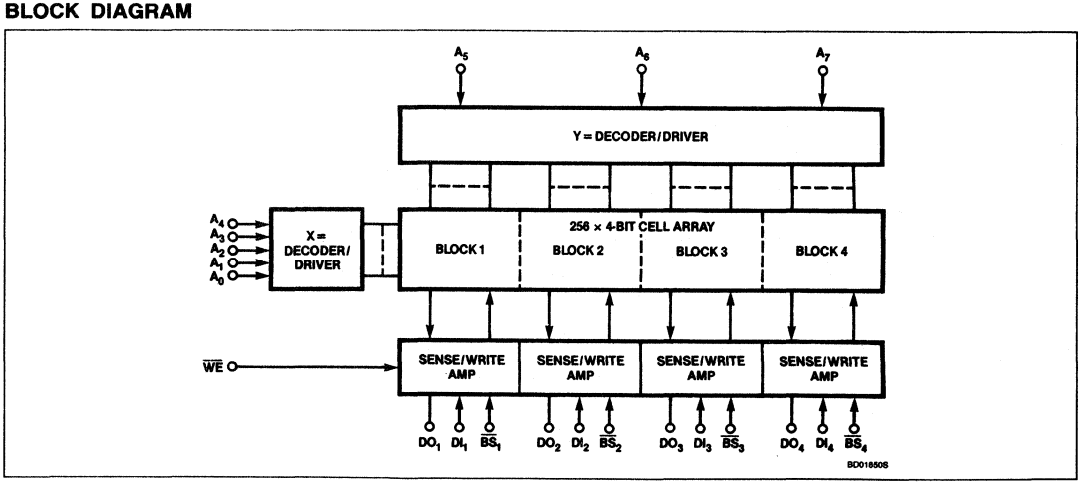
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	+0.5 to −7	V_{dc}
V_{IN}	Input voltage	0 to V_{EE}	V_{dc}
I_O	Output current	−30	mA
T_A	Operating	0 to +85	°C
T_J	Operating junction	+125	°C
T_{STG}	Storage	−55 to +150	°C

BLOCK DIAGRAM



1K-Bit ECL Bipolar RAM (256 × 4) 100422C

ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 400mil wide 24-pin	100422C F

DC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V±5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low		−1.810		−1.475	V
V_{IH}	High		−1.165		−0.880	
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810	−1.715	−1.620	
V_{OH}	High	V_{IH} = Max	−1.025	−0.955	−0.880	V
V_{OLT}	Threshold LOW	V_{IL} = Max			−1.610	
V_{OHT}	Threshold HIGH	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	−50			μA
I_{IL}	$\overline{BS}$	V_{IL} = Min	+0.5			
I_{IH}	High	V_{IH} = Max			220	
I_{EE}	Supply current				210	mA

NOTES:
1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V±5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{AA}	Address access time			7	ns
T_{RBS}	Block select recovery time		4		
T_{ABS}	Block select access time		6		
T_{WD}	Write disable time		4		
T_{WPW}	Write pulse width	5			
T_{WR}	Write recovery time		6		
T_{WHA}	Address hold time		1		
T_{WHBS}	Block select hold time		1		
T_{WHD}	Data hold time		1		
T_{WSA}	Address setup time		1		
T_{WSBS}	Block select setup time		1		
T_{WSD}	Data setup time		1		
t_f	Output fall time		2		
t_r	Output rise time		2		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

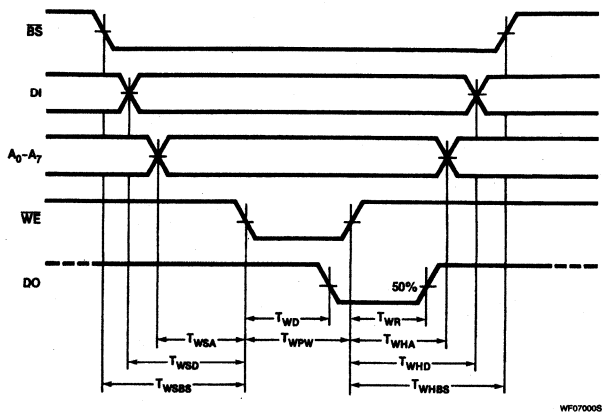
NOTES:
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

TRUTH TABLE

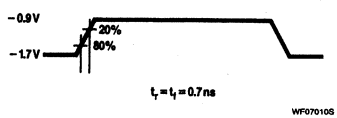
MODE	INPUTS			OUTPUTS
	$\overline{BS_N}$	$\overline{WE}$	DI_N	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
N = Blocks 1 – 4

TIMING DIAGRAMS

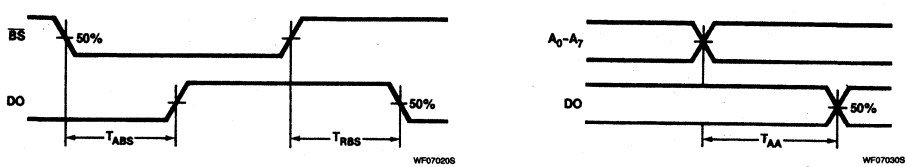


Write Mode



NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels



Read Mode

Signetics

100470A
4K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select Input.

The 100470A is compatible with the 100K ECL families and includes on-chip voltage and temperature compensation.

Ordering information can be found on the following page.

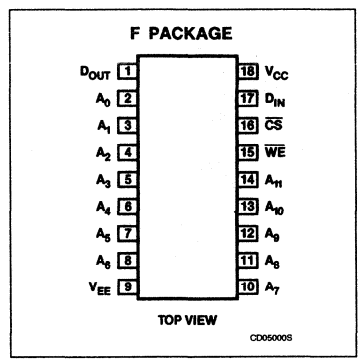
FEATURES

- **Organization: 4096 words by 1 bit**
- **Fully compatible with 100K ECL families**
- **Operating temperature: 0°C to +85°C**
- **Address access time:**
  - **100470A: 15ns max**
- **Low supply current of 150mA max**
- **Read cycle time:**
  - **100470A: 15ns max**

APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

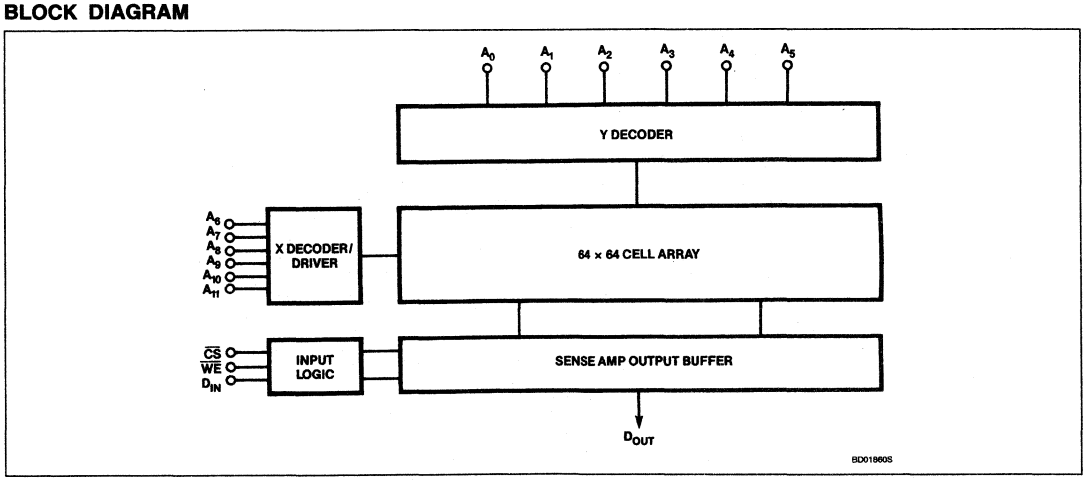
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	+0.5 to −7	V_{dc}
V_{IN}	Input voltage	+0.5 to V_{EE}	
I_O	Output current	−30	mA
T_A	Operating	0 to +85	°C
T_{STG}	Storage	−55 to +150	

BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 300mil wide 18-pin	100470A F

DC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V± 5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low		−1.810		−1.475	V
V_{IH}	High		−1.165		−0.880	
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810	−1.715	−1.620	
V_{OH}	High	V_{IH} = Max	−1.025	−0.955	−0.880	V
V_{OLT}	Threshold LOW	V_{IL} = Max			−1.610	
V_{OHT}	Threshold HIGH	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	−50			μA
I_{IL}	$\overline{CS}$	V_{IL} = Min	+0.5			
I_{IH}	High	V_{IH} = Max			220	
I_{EE}	Supply current				150	mA

NOTES:
1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V± 5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{AA}	Address access time			15	ns
T_{RCS}	Chip select recovery time			5	
T_{ACS}	Chip select access time			5	
T_{WD}	Write disable time			6	
T_{WPW}	Write pulse width	10			
T_{WR}	Write recovery time			10	
T_{WHA}	Address hold time	3			
T_{WHCS}	Chip select hold time	3			
T_{WHD}	Data hold time	3			
T_{WSA}	Address setup time	3			
T_{WSCS}	Chip select setup time	3			
T_{WSD}	Data setup time	3			
t_f	Output fall time		1.5		
t_r	Output rise time		1.5		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

NOTES:
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

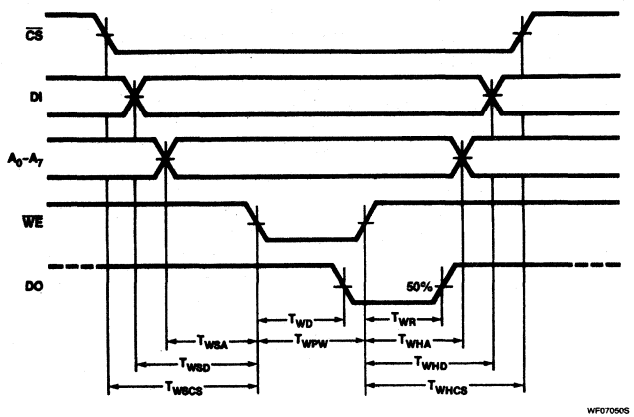
4K-Bit ECL Bipolar RAM (4096 × 1) 100470A

TRUTH TABLE

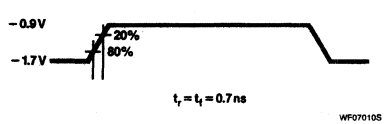
MODE	INPUTS			OUTPUTS
	$\overline{CS}$	$\overline{WE}$	D_{IN}	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care

TIMING DIAGRAMS

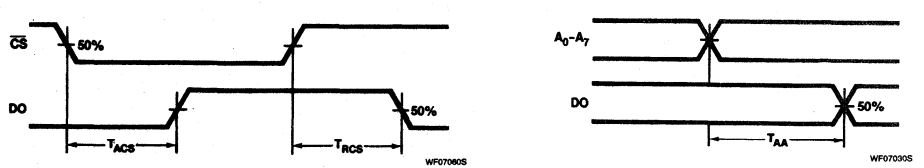


Write Mode



NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels



Read Mode

Signetics

100474A
4K-Bit ECL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100474A device is a 1024 words by 4 bits fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines.

The 100474A, with its voltage and temperature compensation, is compatible with the 100K ECL families.

Ordering information can be found on the following page.

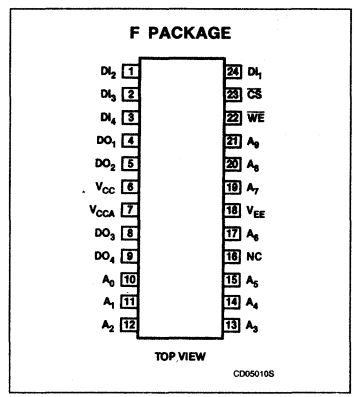
FEATURES

- **Organization: 1024 words by 4 bits**
- **Fully compatible with 100K ECL families**
- **Operating temperature: 0°C to +85°C**
- **Address access time:**
  - **100474A: 15ns max**
- **Low supply current of 210mA max**
- **Read Cycle time:**
  - **100474A: 15ns**

APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

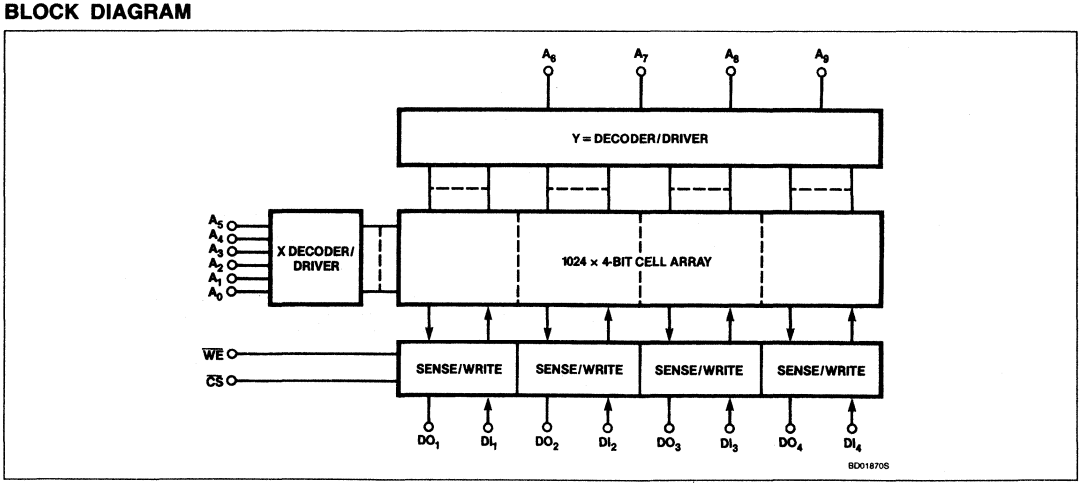
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	+0.5 to −7	V_{dc}
V_{IN}	Input voltage	+0.5 to V_{EE}	
I_O	Output current	−30	mA
T_A	Operating	0 to +85	°C
T_{stg}	Storage	−55 to +150	

BLOCK DIAGRAM



ORDERING CODE

DESCRIPTION	ORDER CODE
Ceramic Dual Inline 400mil wide 24-pin	100474A F

DC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V±5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low		−1.810		−1.475	V
V_{IH}	High		−1.165		−0.880	
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810	−1.715	−1.620	
V_{OH}	High	V_{IH} = Max	−1.025	−0.955	−0.880	V
V_{OLT}	Threshold LOW	V_{IL} = Max			−1.610	
V_{OHT}	Threshold HIGH	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	−50			μA
I_{IL}	$\overline{BS}$	V_{IL} = Min	+0.5			
I_{IH}	High	V_{IH} = Max			220	
I_{EE}	Supply current				210	mA

NOTES:
1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = −4.5V±5%, R_L = 50Ω to −2V, T_A = 0°C to 85°C

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_{AA}	Address access time			15	ns
T_{RCS}	Chip select recovery time			5	
T_{ACS}	Chip select access time			5	
T_{WD}	Write disable time			6	
T_{WPW}	Write pulse width	10			
T_{WR}	Write recovery time			10	
T_{WHA}	Address hold time	3			
T_{WHCS}	Chip select hold time	3			
T_{WHD}	Data hold time	3			
T_{WSA}	Address setup time	3			
T_{WSCS}	Chip select setup time	3			
T_{WSD}	Data setup time	3			
t_f	Output fall time		1.5		
t_r	Output rise time		1.5		
Capacitance					pF
C_{IN}	Input			8	
C_{OUT}	Output			8	

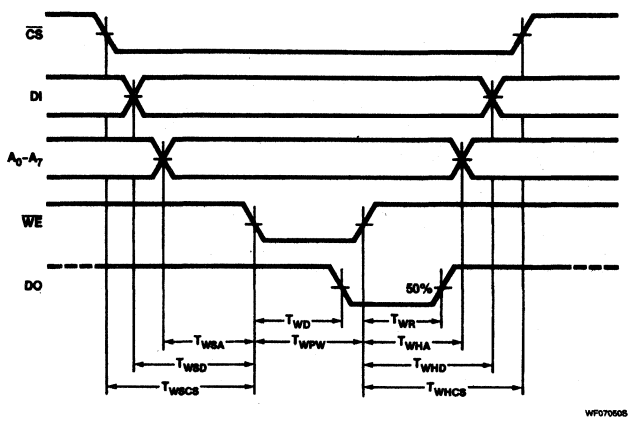
NOTES:
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

TRUTH TABLE

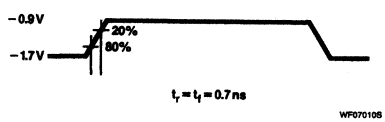
MODE	INPUTS			OUTPUTS
	$\overline{CS}$	$\overline{WE}$	D_{IN}	
Disable	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care

TIMING DIAGRAMS

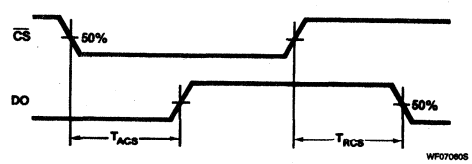


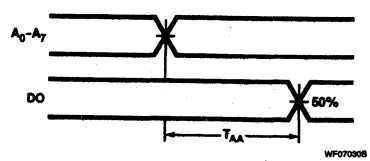
Write Mode



NOTE:
All timing measurements referenced to 50% of input levels.

Input Levels





Read Mode

Bipolar ECL PROM

Signetics

10149
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149 is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

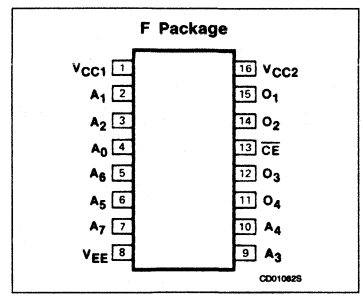
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

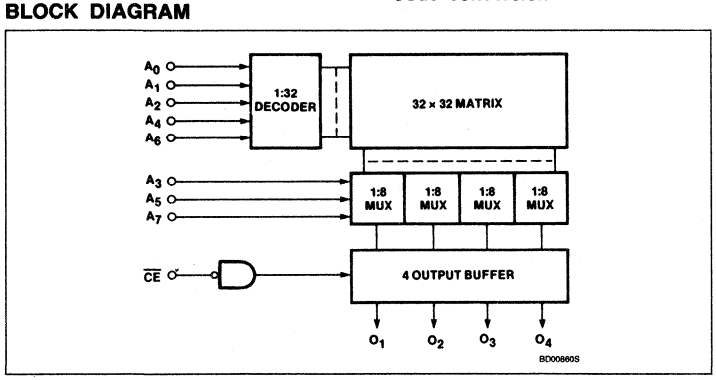
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit ECL Bipolar PROM (256 × 4) 10149

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP 300mil-wide	10149 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
	Temperature range		
T_A	Operating	−30 to +85	°C
T_{STG}	Storage	−55 to +165	

DC ELECTRICAL CHARACTERISTICS $-30°C \leq T_A < +85°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER[1]	TEST CONDITIONS	−30°C		+25°C			+85°C		UNIT
			Min	Max	Min	Typ[3]	Max	Min	Max	
Input voltage[2,3]										
V_{IL}	Low		−1.890		−1.850			−1.825		
V_{IH}	High			−0.890			−0.810		−0.700	V
V_{ILA}	Low threshold			−1.500			−1.475		−1.440	
V_{IHA}	High threshold		−1.205		−1.105			−1.035		
Output voltage										
V_{OL}	Low	V_{IH} = Max	−1.89	−1.675	−1.85		−1.65	−1.825	−1.615	
V_{OH}	High	V_{IL} = Min	−1.06	−0.89	−0.96		−0.81	−0.89	−0.70	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		−1.655			−1.63		−1.595	
V_{OHA}	High threshold		−1.08		−0.98			−0.91		
Input current										
I_{IL}	Low	V_{IH} = Max			0.5					μA
I_{IH}	High	V_{IL} = Min		250			250		250	
Supply drain current										
I_{EE}		V_{EE} = −5.2V		160		150	160		160	mA

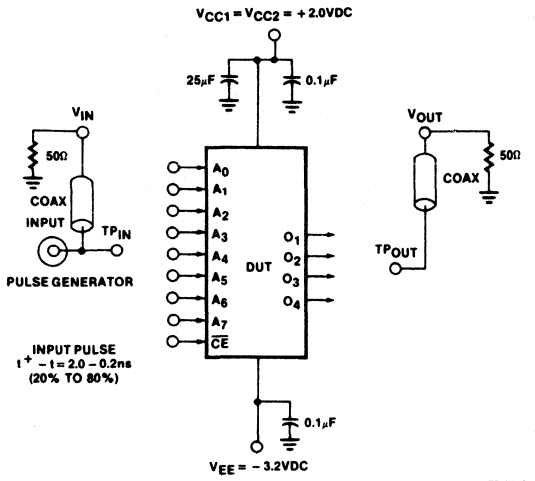
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, C_L = 30pF, $-30°C \leq T_A \leq +85°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
Access time							
t_{AA}		Output	Address		14	20	ns
t_{CE}		Output	Chip enable		4	8	
Disable time							
t_{CD}		Output	Chip enable		4	8	ns
Rise and fall time							
t_+	Rise time (20-80%)				4.0		ns
t_-	Fall time (80-20%)				4.0		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. Typical values are at V_{EE} = −5.2V, T_A = +25°C.

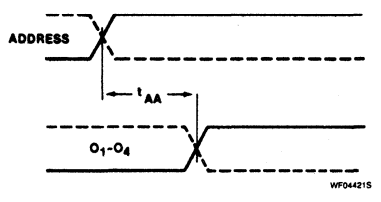
TEST LOAD CIRCUIT



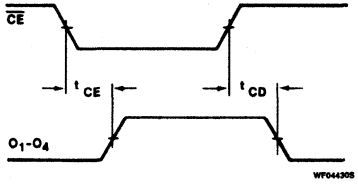
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORM



Address Access Time



Chip Enable/Disable Propagation Delays

Signetics

10149A
1K-Bit ECL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10149A is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the folowing page.

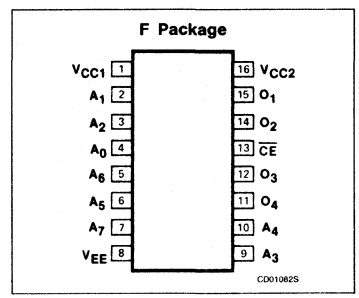
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

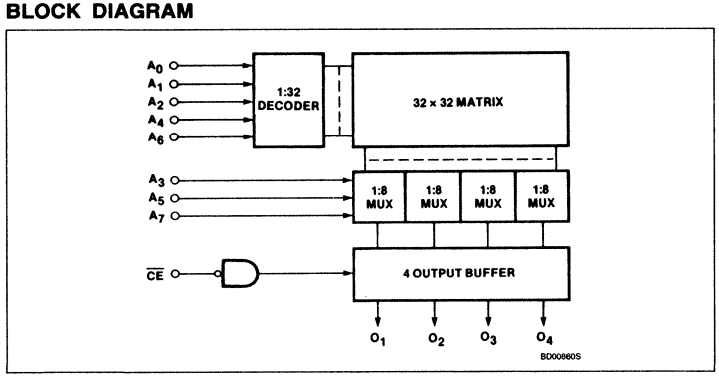
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit ECL Bipolar PROM (256 × 4) — 10149A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP 300mil-wide	10149A F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
	Temperature range		
T_A	Operating	−30 to +85	°C
T_{STG}	Storage	−55 to +165	

DC ELECTRICAL CHARACTERISTICS −30°C ≤ T_A < +85°C, −4.94V ≤ V_{EE} ≤ −5.46V

SYMBOL	PARAMETER[1]	TEST CONDITIONS	−30°C		+25°C			+85°C		UNIT
			Min	Max	Min	Typ[3]	Max	Min	Max	
Input voltage[2,3]										
V_{IL}	Low		−1.890		−1.850			−1.825		V
V_{IH}	High			−0.890			−0.810		−0.700	
V_{ILA}	Low threshold			−1.500			−1.475		−1.440	
V_{IHA}	High threshold		−1.205		−1.105			−1.035		
Output voltage										
V_{OL}	Low	V_{IH} = Max	−1.89	−1.675	−1.85		−1.65	−1.825	−1.615	V
V_{OH}	High	V_{IL} = Min	−1.06	−0.89	−0.96		−0.81	−0.89	−0.70	
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		−1.655			−1.63		−1.595	
V_{OHA}	High threshold		−1.08		−0.98			−0.91		
Input current										
I_{IL}	Low	V_{IH} = Max			0.5					μA
I_{IH}	High	V_{IL} = Min		250			250		250	
Supply drain current										
I_{EE}		V_{EE} = −5.2V		160		150	160		160	mA

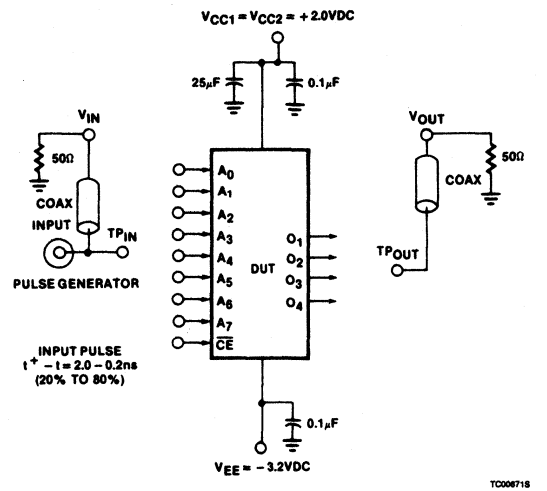
AC ELECTRICAL CHARACTERISTICS R_1 = 50Ω, C_L = 30pF, −30°C ≤ T_A ≤ +85°C, −4.94V ≤ V_{EE} ≤ −5.46V

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
Access time							
t_{AA}		Output	Address			10	ns
t_{CE}		Output	Chip enable		4	6	
Disable time							
t_{CD}		Output	Chip enable		4	6	ns
Rise and fall time							
t_+	Rise time (20-80%)				4.0		ns
t_-	Fall time (80-20%)				4.0		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. Typical values are at V_{EE} = −5.2V, T_A = +25°C.

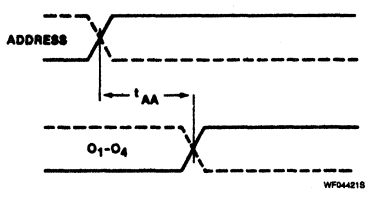
TEST LOAD CIRCUIT



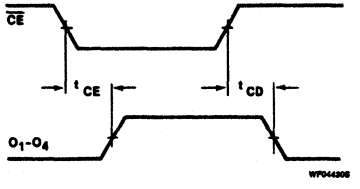
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORM



Address Access Time



Chip Enable/Disable Propagation Delays

Signetics

100149
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 100149 is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 100149 is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

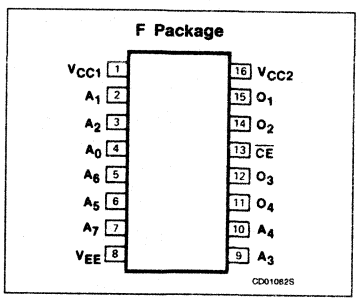
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

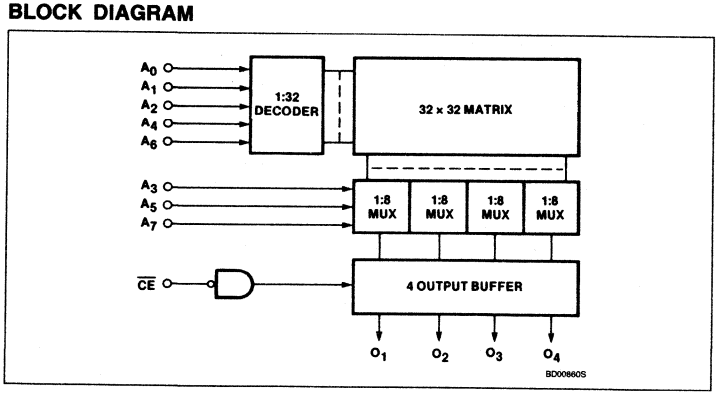
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit ECL Bipolar PROM (256 × 4) — 100149

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP 300mil-wide	100149 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
	Temperature Range		
T_A	Operating	−0 to +75	°C
T_{STG}	Storage	−55 to +165	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		−1.810			
V_{IH}	High				−0.880	V
V_{ILA}	Threshold Low				−1.475	
V_{IHA}	Threshold High		−1.165			
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810		−1.620	
V_{OH}	High	V_{IH} = Max	−1.025		−0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			−1.610	
V_{OHA}	Threshold High	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	0.5			μA
I_{IH}	High	V_{IH} = Max			220	
Supply current						
I_{EE}		V_{EE} = −4.5V		150	180	mA

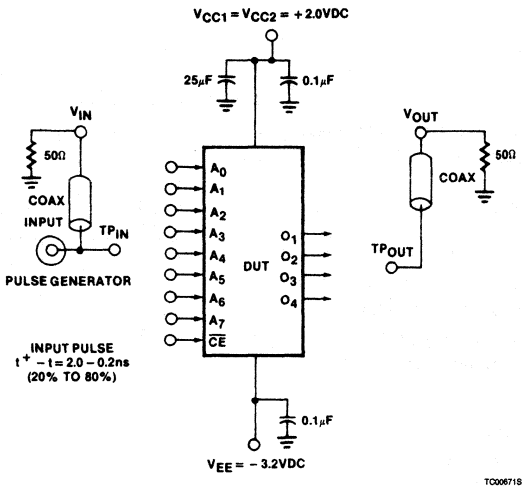
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, C_L = 30pF, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time							
t_{AA}		Output	Address		15	20	ns
t_{CE}		Output	Chip enable		5	8	
Disable time							
t_{CD}		Output	Chip disable		5	8	ns
Rise and fall time							
t^+	Rise time (20-80%)				4.0		ns
t^-	Fall time (80-20%)				4.0		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = −4.5V, T_A = +25°C.

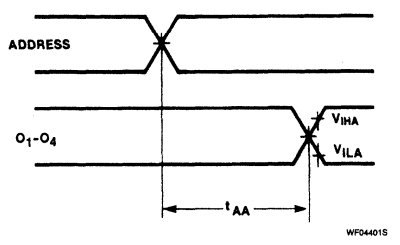
TEST LOAD CIRCUIT



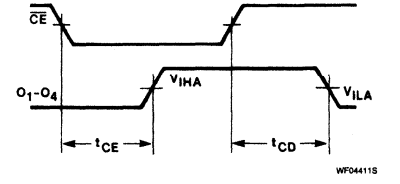
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORM



Address Access Time



Chip Enable/Disable Propagation Delays

Signetics

100149A
1K-Bit ECL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100149A is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 100149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

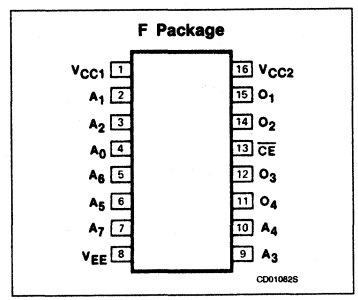
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

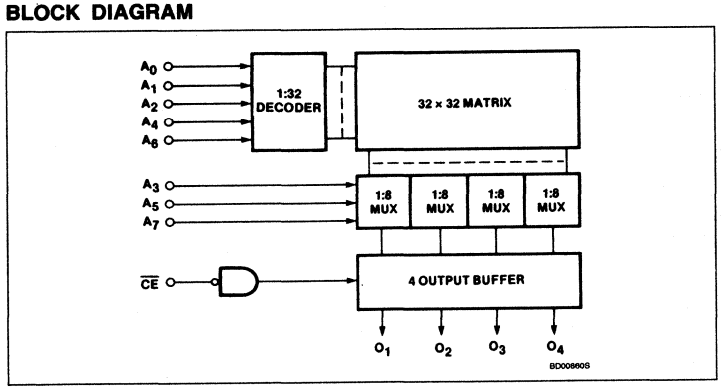
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit ECL Bipolar PROM (256 × 4) — 100149A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP 300mil-wide	100149A F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
	Temperature Range		
T_A	Operating	−0 to +75	°C
T_{STG}	Storage	−55 to +165	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		−1.810			
V_{IH}	High				−0.880	V
V_{ILA}	Threshold Low				−1.475	
V_{IHA}	Threshold High		−1.165			
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810		−1.620	
V_{OH}	High	V_{IH} = Max	−1.025		−0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			−1.610	
V_{OHA}	Threshold High	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	0.5			μA
I_{IH}	High	V_{IH} = Max			220	
Supply current						
I_{EE}		V_{EE} = −4.5V		150	160	mA

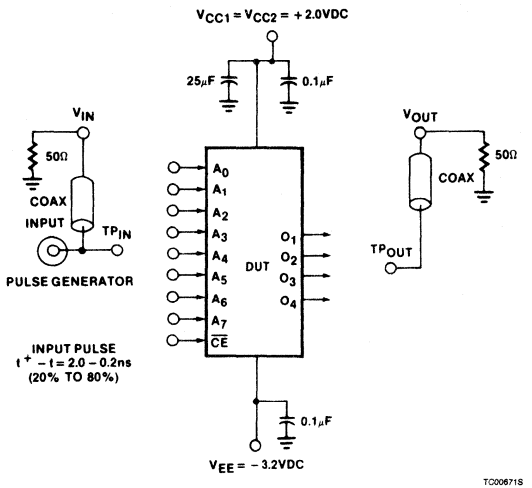
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, C_L = 30pF, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time							
t_{AA}		Output	Address			10	ns
t_{CE}		Output	Chip enable		5	6	
Disable time							
t_{CD}		Output	Chip disable		5	6	ns
Rise and fall time							
t^+	Rise time (20-80%)				4.0		ns
t^-	Fall time (80-20%)				4.0		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = −4.5V, T_A = +25°C.

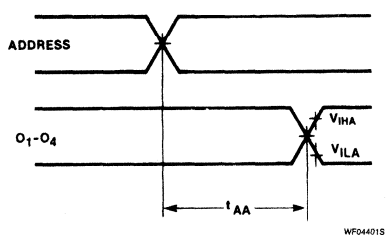
TEST LOAD CIRCUIT



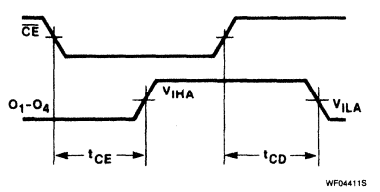
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORM



Address Access Time



Chip Enable/Disable Propagation Delays

PACKAGE INFORMATION

Package Outlines

Package Outlines

Bipolar Memory Products

INTRODUCTION

The following information applies to packages currently used for Bipolar Memories. For information on other package configurations, refer to the respective Data Manual for each product.

GENERAL

1. The following pages contain information on plastic DIP and cerdip packages ranging from 16 pins to 28 pins, the SO-L 16- and 20-pin and the 28-pin Leaded Chip Carrier.
2. Information for each set of drawings such as notes and reference standards are included on each drawing for easy reference.
3. Thermal resistance values have been determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. Since thermal resistance values are dependent on die size and the value of power dissipated, measurements were made on packages containing various die sizes. The information in the tables shown here are typical values for a mid bipolar memory die size for a given package. For more detailed information on thermal performance of specific packages please contact your Signetics sales representative and request the latest publication of Thermal Performance Data.

Package Outlines

PLASTIC PLCC

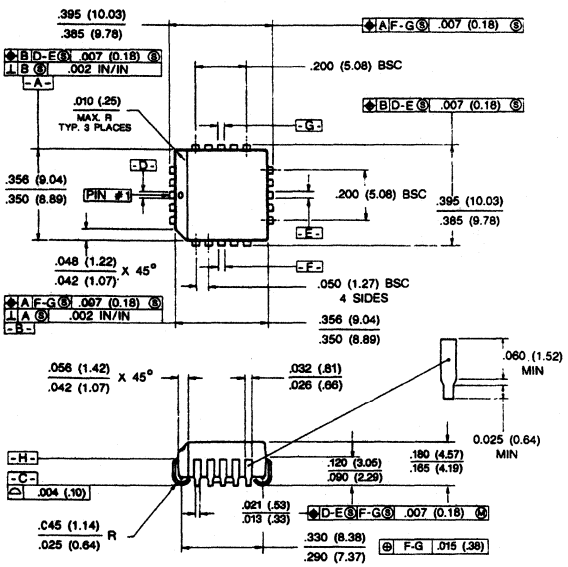
1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test Fixture: Device soldered to a glass epoxy test board with the dimensions 1.58″ × 0.75″ × 0.059″ with 0.009″ stand off.

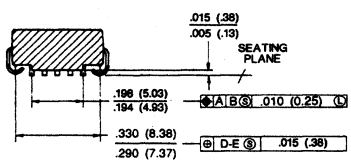
PLASTIC LEADED CHIP CARRIER

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
20	A	60/24	350mil-square
28	A		450mil-square

Package Outlines

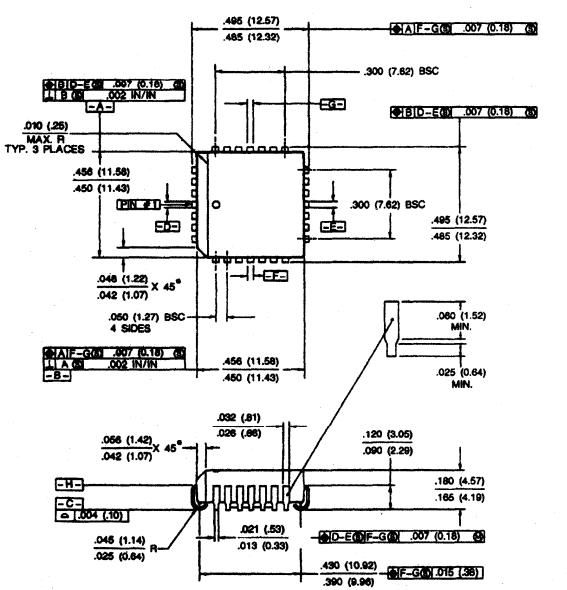
20-PIN PLASTIC LEADED CHIP CARRIER

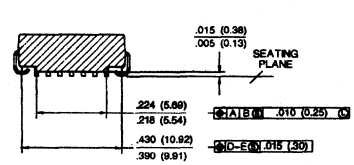




NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #20 (top view).

28-PIN PLASTIC LEADED CHIP CARRIER





NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).

Package Outlines

PLASTIC SO-L

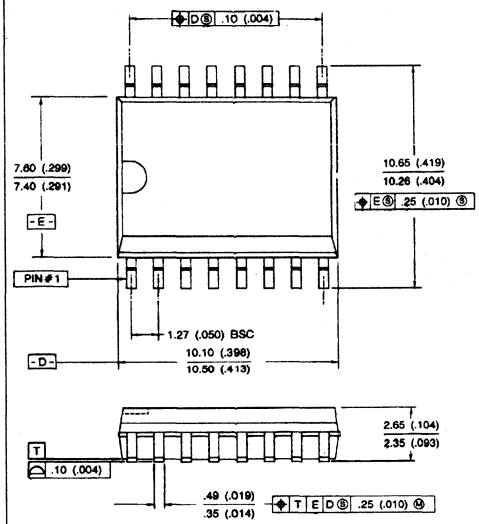
1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test fixture: Device soldered to a glass epoxy test board with the dimensions of 1.58″ × 0.75″ × 0.059″ with 0.009″ stand off.

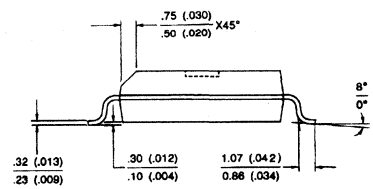
PLASTIC SMALL OUTLINE PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	D	95/30	300mil-wide
20	D	86/24	300mil-wide

Package Outlines

16-PIN SMALL OUTLINE



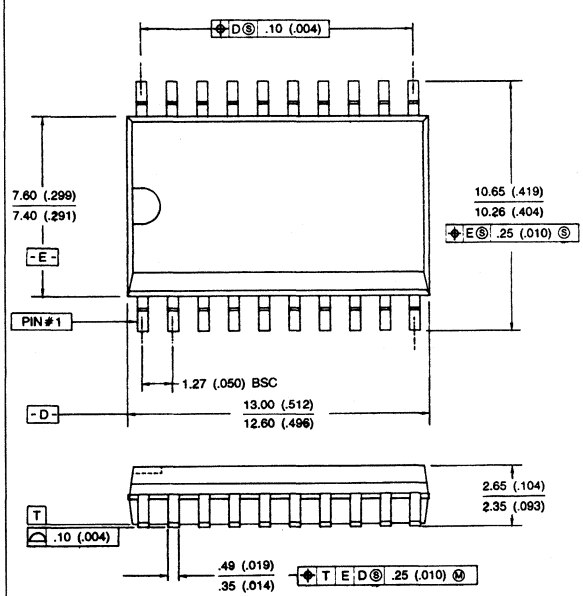


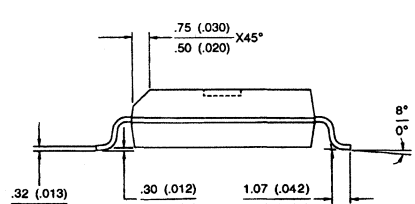
853-0171 81216

PO00242S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.

20-PIN SMALL OUTLINE





853-0172 81219

PO00231S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.

Package Outlines

CERAMIC DIP

1. Lead material: ASTM alloy F-30 (Alloy 42) or equivalent – tin plated or solder dipped.
2. Body Material: Ceramic with glass seal at leads.
3. Thermal test fixture: Device secured in Textool ZIF socket with 0.04" stand off.

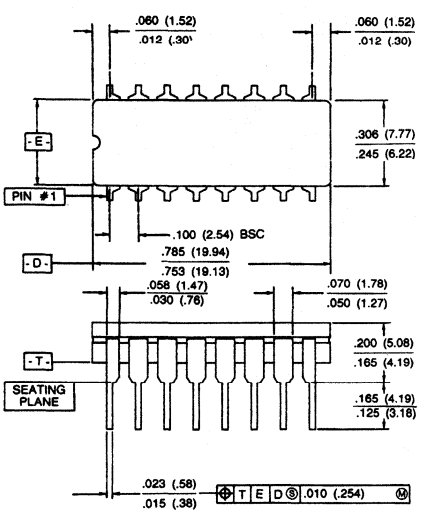
CERAMIC DUAL-IN-LINE PACKAGES

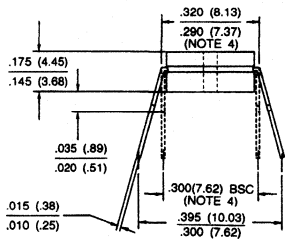
NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	F	77/30	300mil-wide
18	F	73/27	300mil-wide
20	F	72/25	300mil-wide
22	F	66/27	400mil-wide
24	F/F3[1]	63/26	300mil-wide
24	F	62/26	600mil-wide
28	F	57/27	600mil-wide

NOTES:
1. Order coded as F3 when both 600 and 300mil-wide packages are available.

Package Outlines

16-PIN CERAMIC DIP



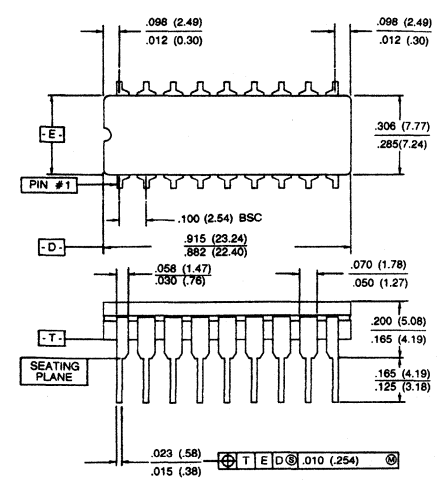


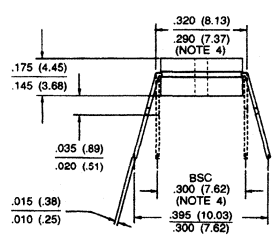
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0582 81594

PO00490S

18-PIN CERAMIC DIP





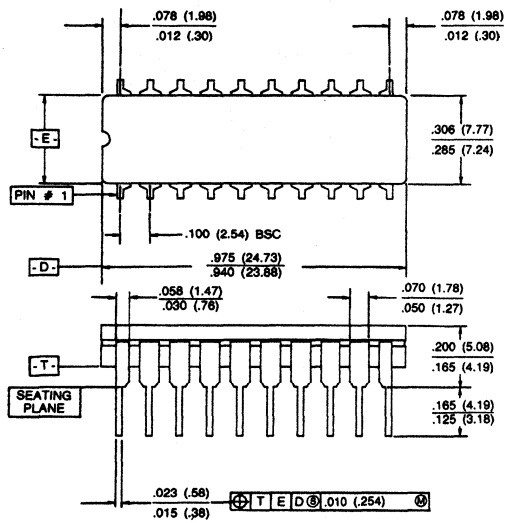
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

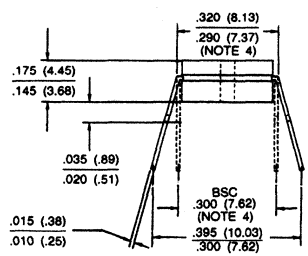
853-0583 81594

PO00470S

Package Outlines

20-PIN CERAMIC DIP



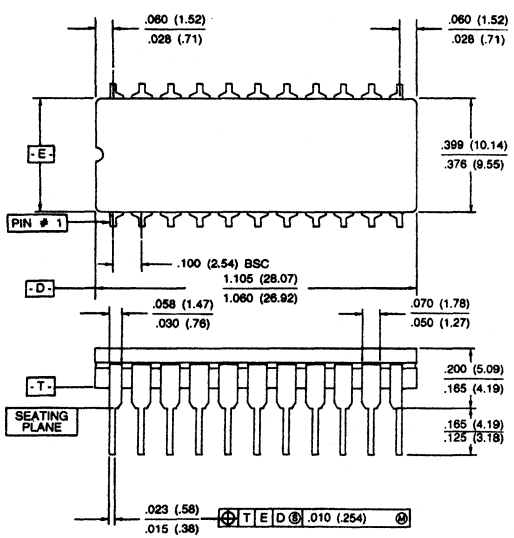


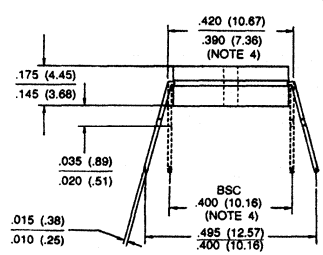
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0584 81594

PO00430S

22-PIN CERAMIC DIP





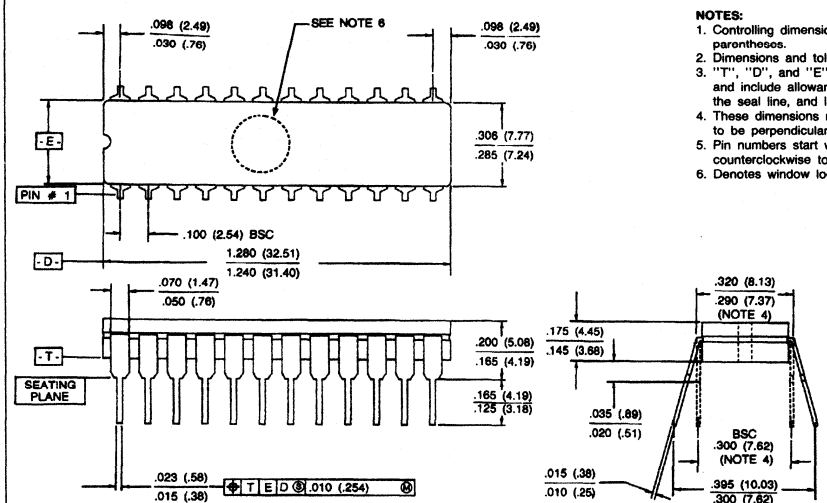
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

853-0585 81594

PO00420S

Package Outlines

24-PIN CERAMIC DIP (300mil-wide)

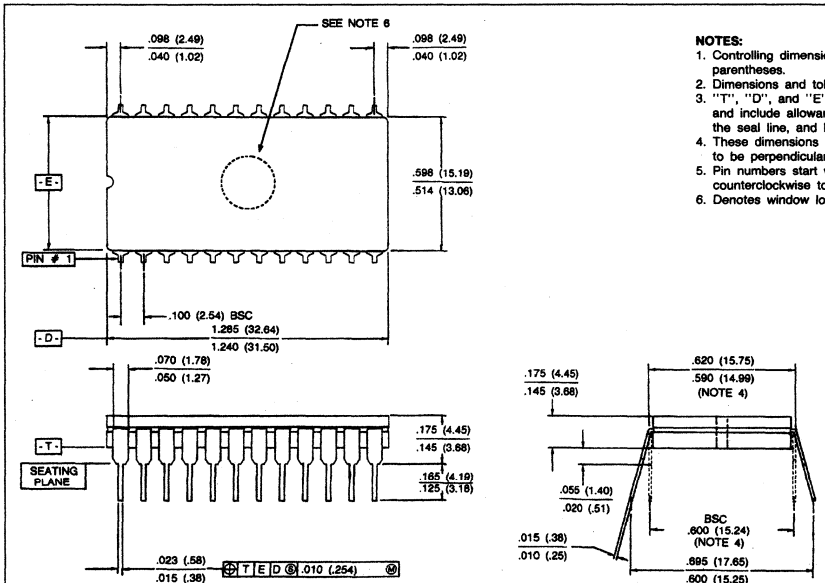


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

853-0586 84000

PO00402S

24-PIN CERAMIC DIP (600mil-wide)



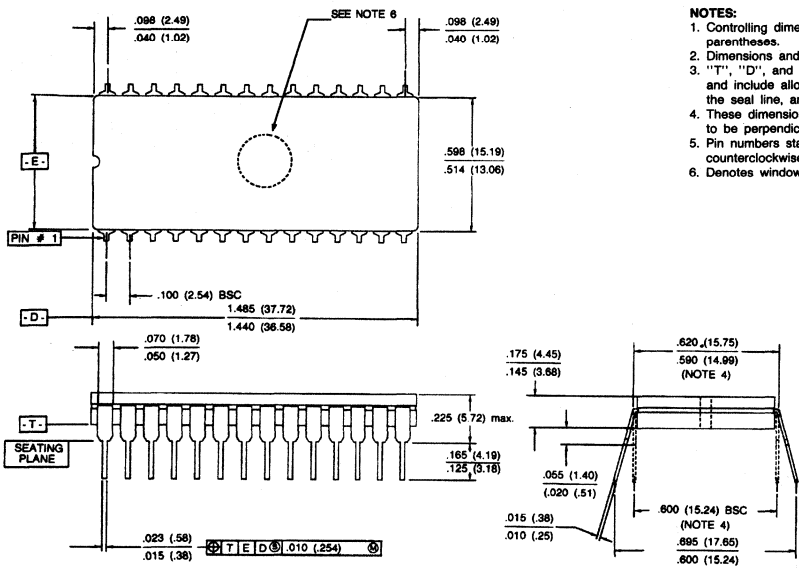
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

853-0588 84221

PO00462S

Package Outlines

28-PIN CERAMIC DIP



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM products.

853-0589 84000

P000391S

Package Outlines

PLASTIC DIP

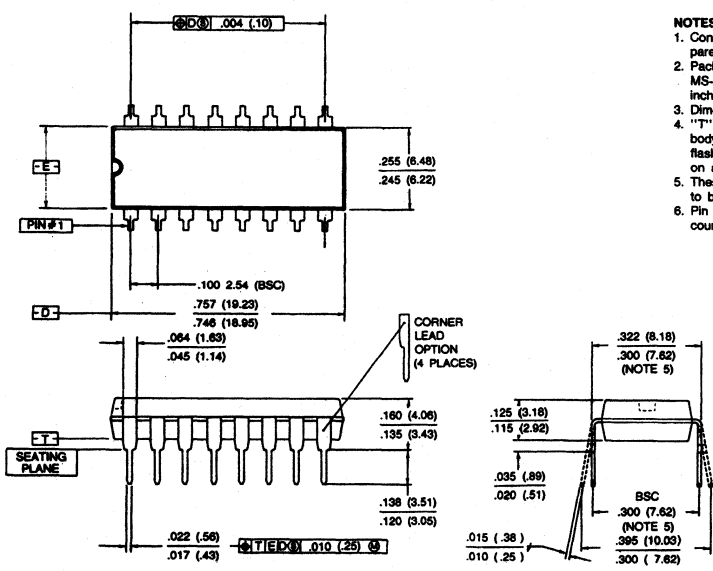
1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test fixture: Device secured in a Textool ZIF socket with 0.04" stand off.

PLASTIC DUAL-IN-LINE PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	N	76/26	300mil-wide
18	N	63/24	300mil-wide
20	N	60/24	300mil-wide
22	N	54/20	400mil-wide
24	N/N3[1]	46/18	300mil-wide
24	N	44/18	600mil-wide
28	N	42/16	600mil-wide

NOTES:
1. Order coded as N3 when both 600mil and 300mil-wide packages are available.

16-PIN PLASTIC DIP



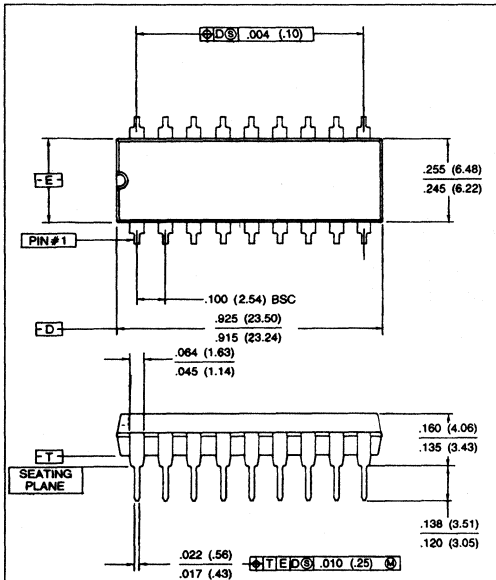
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

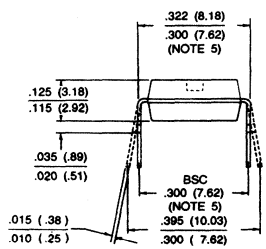
853-0406 81232

PO002805

Package Outlines

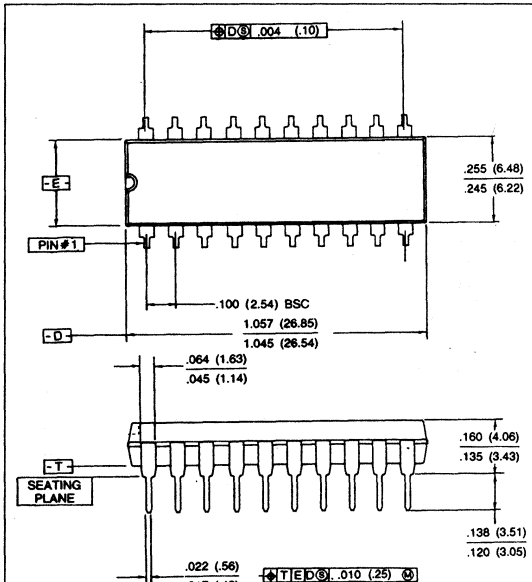
18-PIN PLASTIC DIP

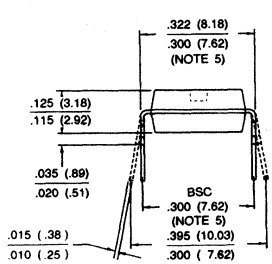




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AD for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

20-PIN PLASTIC DIP

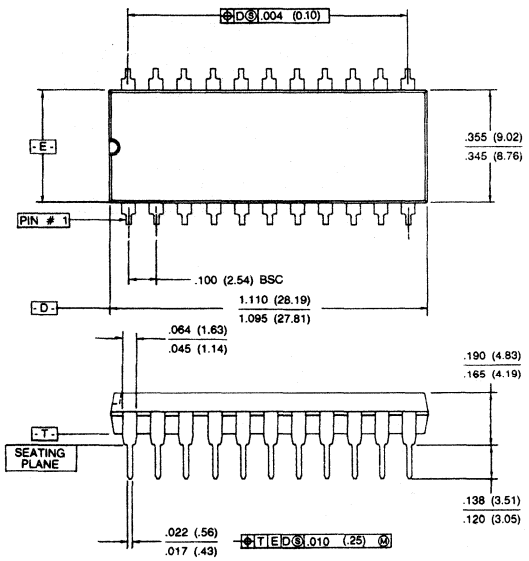




NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

Package Outlines

22-PIN PLASTIC DIP

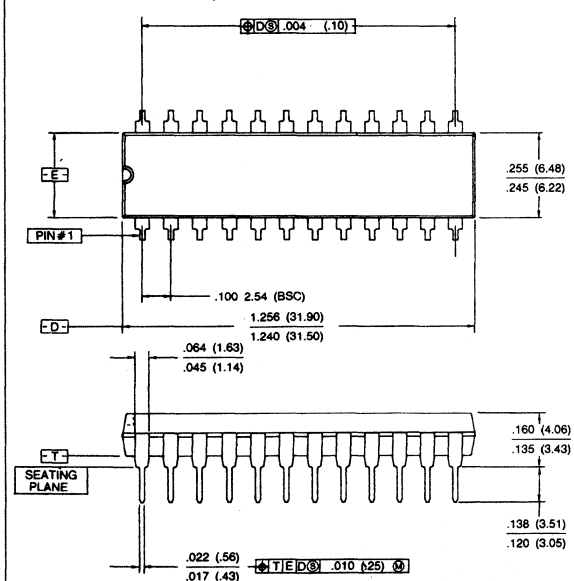


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-010-AA for standard dual in-line (DIP) package .400 inch row spacing (PLASTIC) 22 leads (issue A. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

853-0409 81235

PO00341S

24-PIN PLASTIC DIP (300mil-wide)



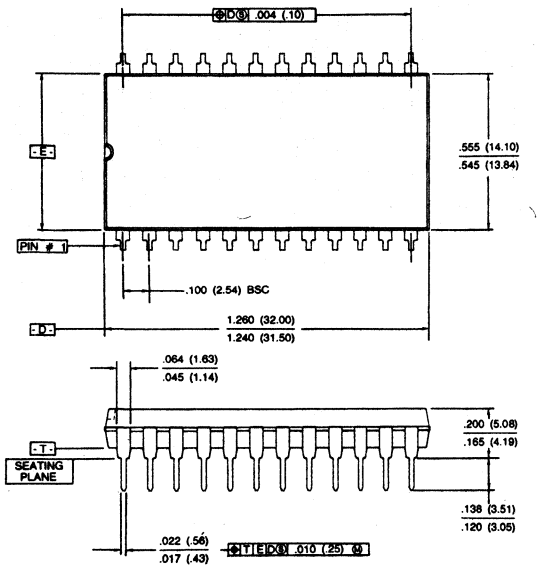
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AR for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0410 81236

PO00320S

Package Outlines

24-PIN PLASTIC DIP (600mil-wide)

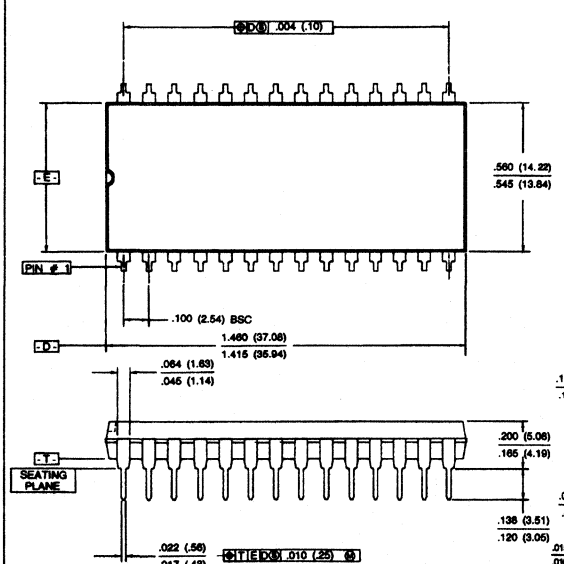


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0412 81238

PO003615

28-PIN PLASTIC DIP



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413 84099

PO003728

Package Outlines

HERMETIC CERDIP WITH QUARTZ WINDOW

1. Package dimensions conform to JEDEC specifications for standard Ceramic Dual Inline (Cerdip) package.
2. Controlling dimensions are given in inches with dimensions in millimeters, mm, contained in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M - 1982.
4. Pin numbers start with pin #1 and continue counterclockwise when viewed from the top.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Lead material: ASTM alloy F-30 (Alloy 42) or equivalent - tin plated or solder dipped.
7. Body Material: Ceramic with glass seal at leads.
8. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. Test condition for these values follow:

   Test Ambient — Still Air

   Test Fixture — θ_{JA} - Textool ZIF socket with 0.04″ standoff

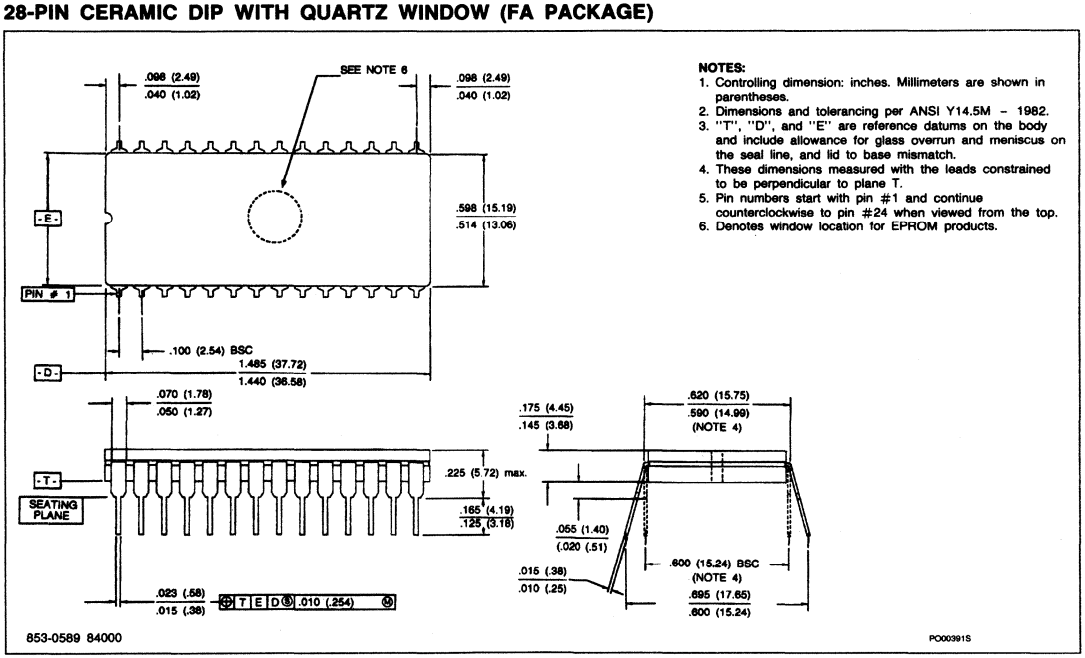
   θ_{JC} - Water cooled heat sink

HERMETIC DUAL-IN-LINE PACKAGES WITH QUARTZ WINDOW

NO. OF LEADS	PACKAGE CODE	DESCRIPTION
24	F	300mil-wide
28	F	600mil-wide

TYPICAL θ_{JA}/θ_{JC} VALUES (°C/W)			
Die Size	Power Dissipation (W)	Average θ_{JA}	Average θ_{JC}
25K	.5	67	7.8
30K	.5	52	7.0

28-PIN CERAMIC DIP WITH QUARTZ WINDOW (FA PACKAGE)



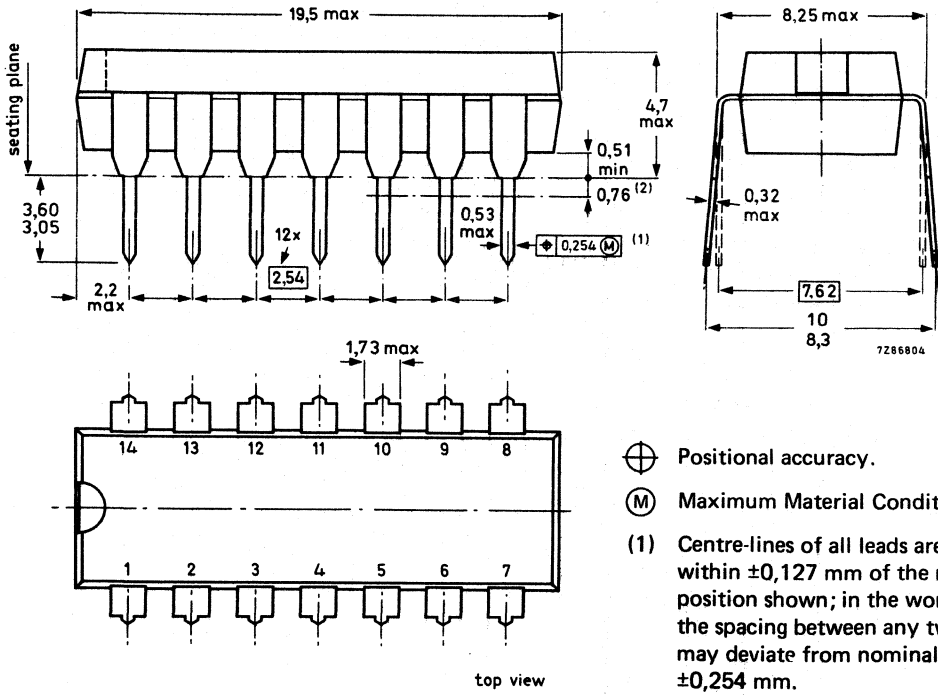
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

Package Outlines

The package information for each type number is given below:

type number	description and package code	page
HEF4505BP	14-lead dual in-line; plastic (SOT-27)	399
HEF4505BD	14-lead dual in-line; ceramic (cerdip) (SOT-73)	401
HEF4720BP	16-lead dual in-line; plastic (SOT-38Z)	400
HEF4720VP	16-lead dual in-line; plastic (SOT-38Z)	400
HEF4720BD	16-lead dual in-line; ceramic (cerdip) (SOT-74)·	402
HEF4720VD	16-lead dual in-line; ceramic (cerdip) (SOT-74)	402
HEF4720BT	16-lead mini-pack; plastic (SO-16L; SOT-162A)	412
HEF4720VT	16-lead mini-pack; plastic (SO-16L; SOT-162A)	412
PCD5101P	22-lead dual in-line; plastic (SOT-116)	407
PCD5101T	24-lead mini-pack; plastic (SO-24; SOT-137A)	410
PCD5114D	18-lead dual in-line; ceramic (cerdip) (SOT-133B)	409
PCD5114P	18-lead dual in-line; plastic (SOT-102G, N, PE)	406
PCD5114T	20-lead mini-pack; plastic (SO-20; SOT-163A)	413
PCF8570P	8-lead dual in-line; plastic (SOT-97)	404
PCF8570T	8-lead mini-pack; plastic (SO-8L; SOT-176)	414
PCF8571D	8-lead dual in-line; ceramic (cerdip) (SOT-151A)	411
PCF8571P	8-lead dual in-line; plastic (SOT-97)	404
PCF8571T	8-lead mini-pack; plastic (SO-8L; SOT-176)	414
PCF8582P	8-lead dual in-line; plastic (SOT-97)	404
PCF8583P	8-lead dual in-line; plastic (SOT-97)	404
PCF8583T	8-lead mini-pack; plastic (SO-8L; SOT-176)	414
SAA9001PB	28-lead dual in-line; plastic (SOT-117)	408
SAA9001EB	28-lead dual in-line; metal ceramic (cerdil) (SOT-87B)	403
SBB6116P	24-lead dual in-line; plastic (SOT-101A, B, F, G, L)	405

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27)



Dimensions in mm

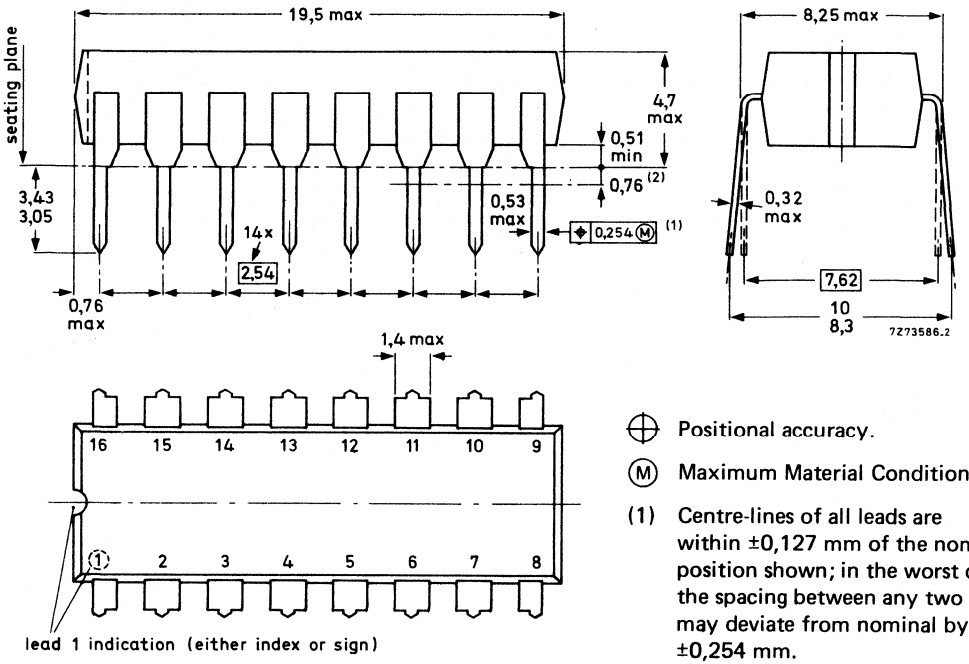
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

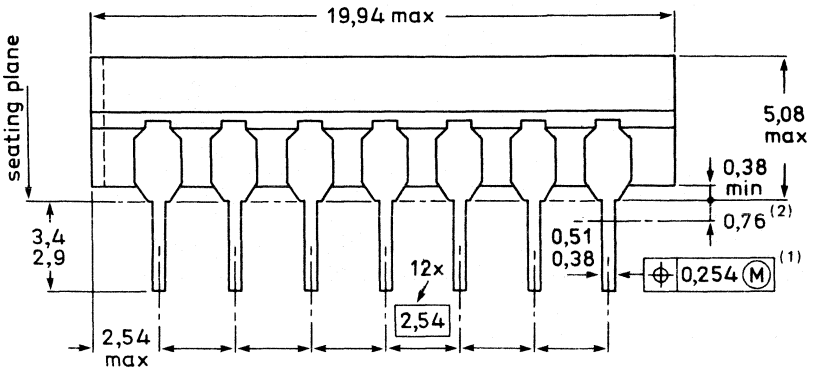
Ⓜ Maximum Material Condition.

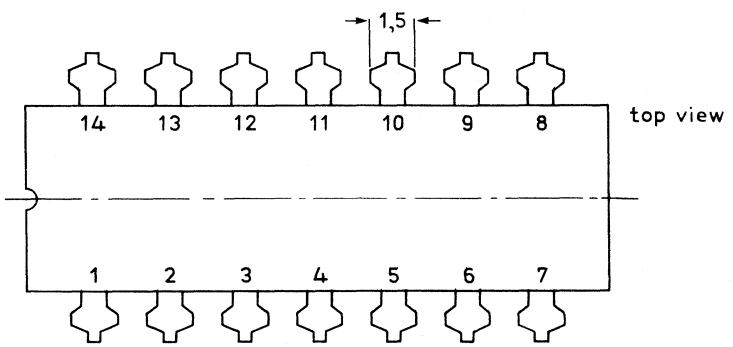
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

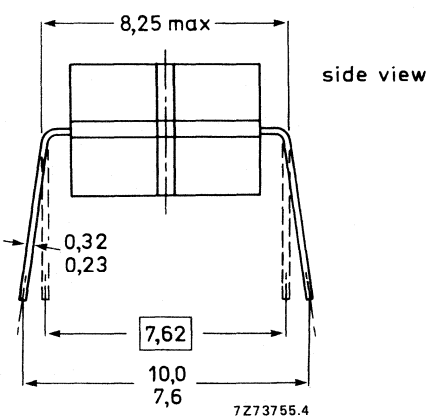
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

14-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-73)







⊕ Positional accuracy.

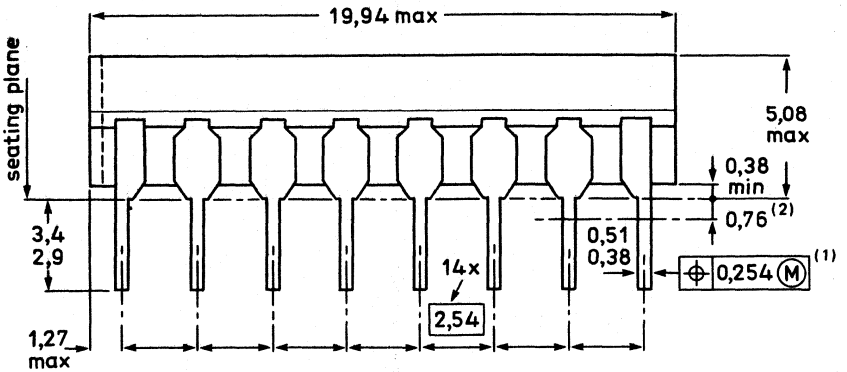
Ⓜ Maximum Material Condition.

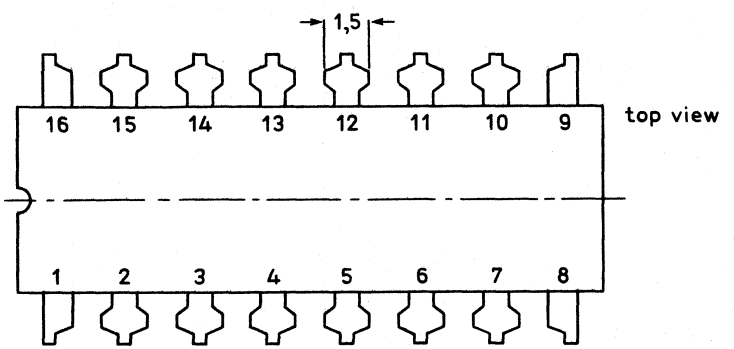
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

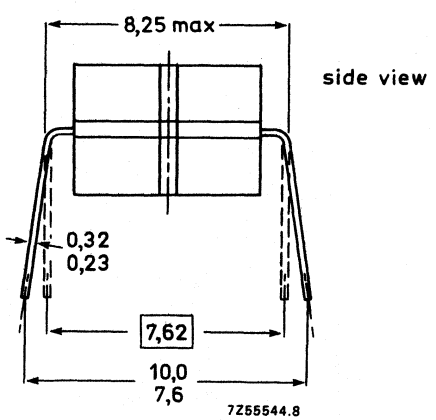
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-74)







⊕ Positional accuracy.

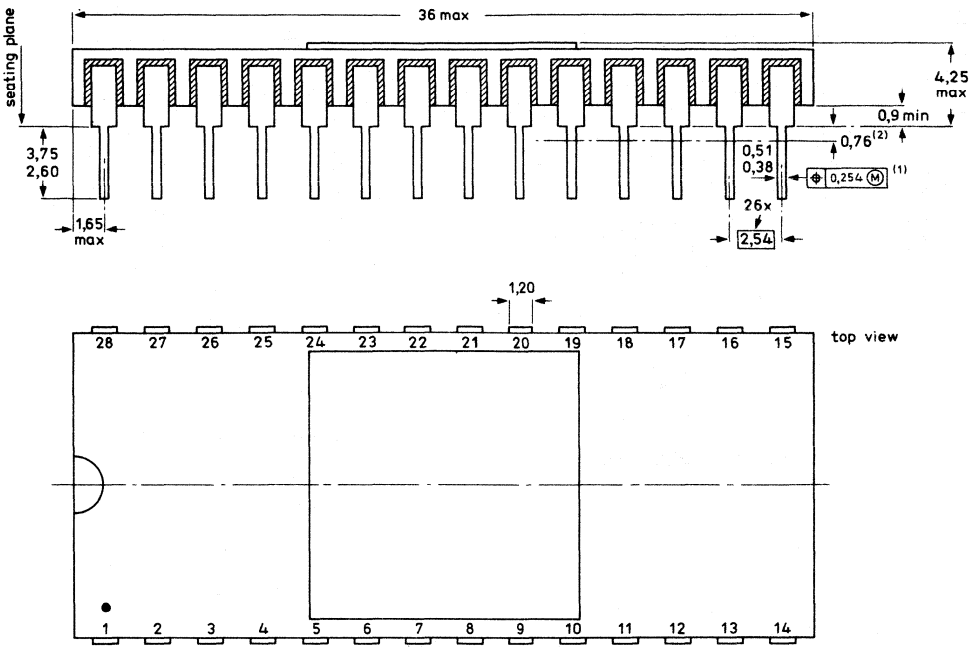
Ⓜ Maximum Material Condition.

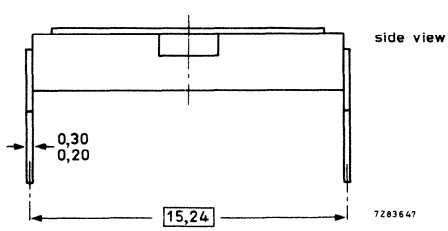
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-87B)





Dimensions in mm

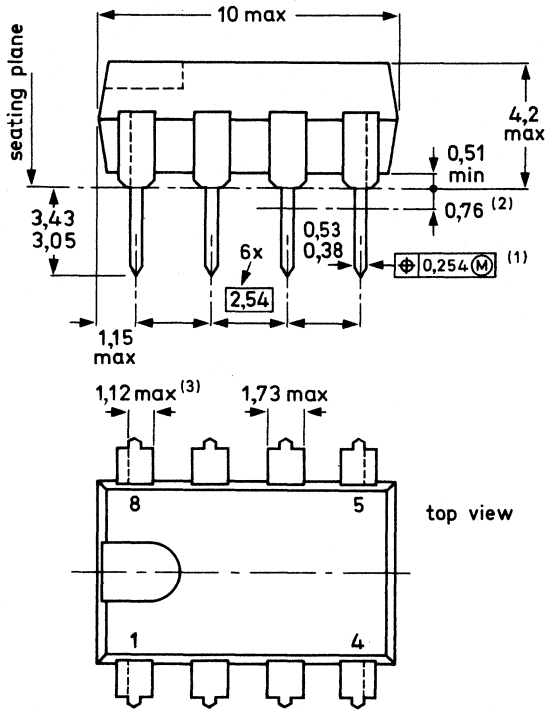
⊕ Positional accuracy.

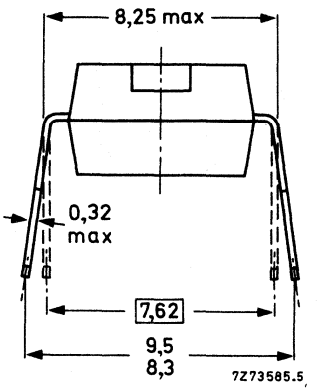
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97)





Dimensions in mm

⊕ Positional accuracy.

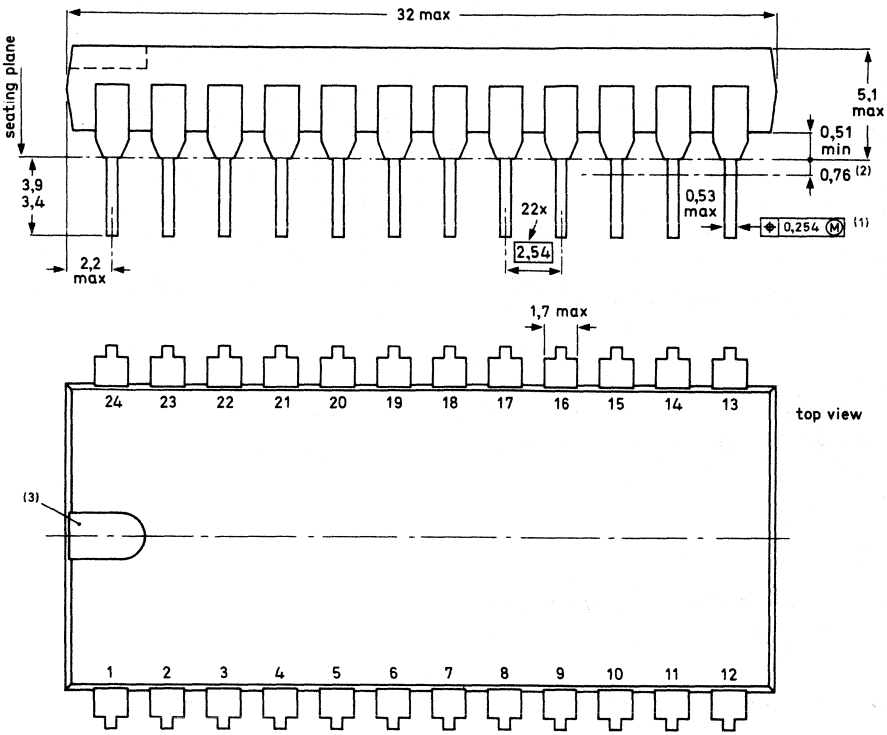
Ⓜ Maximum Material Condition.

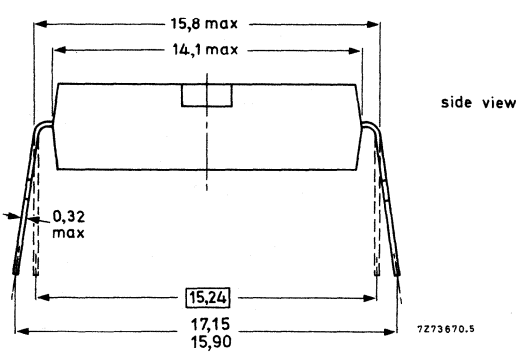
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A,B,F,G,L)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

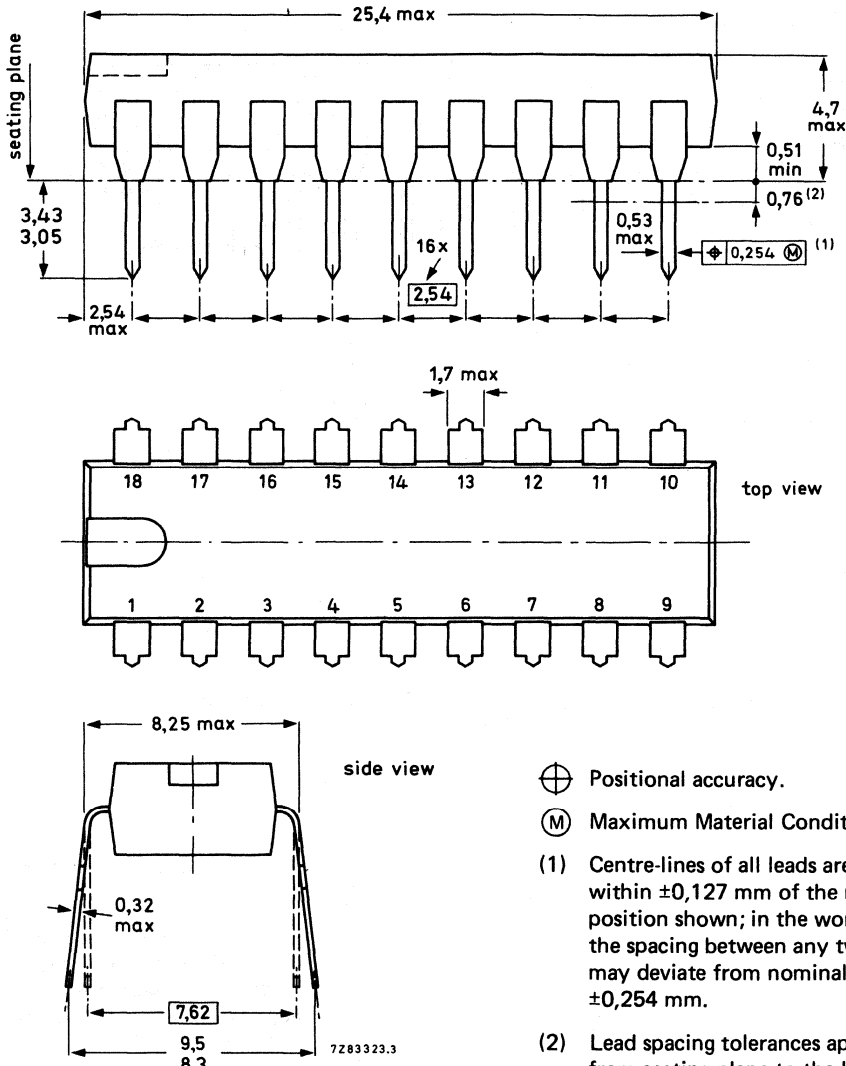
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G,N,PE)



⊕ Positional accuracy.

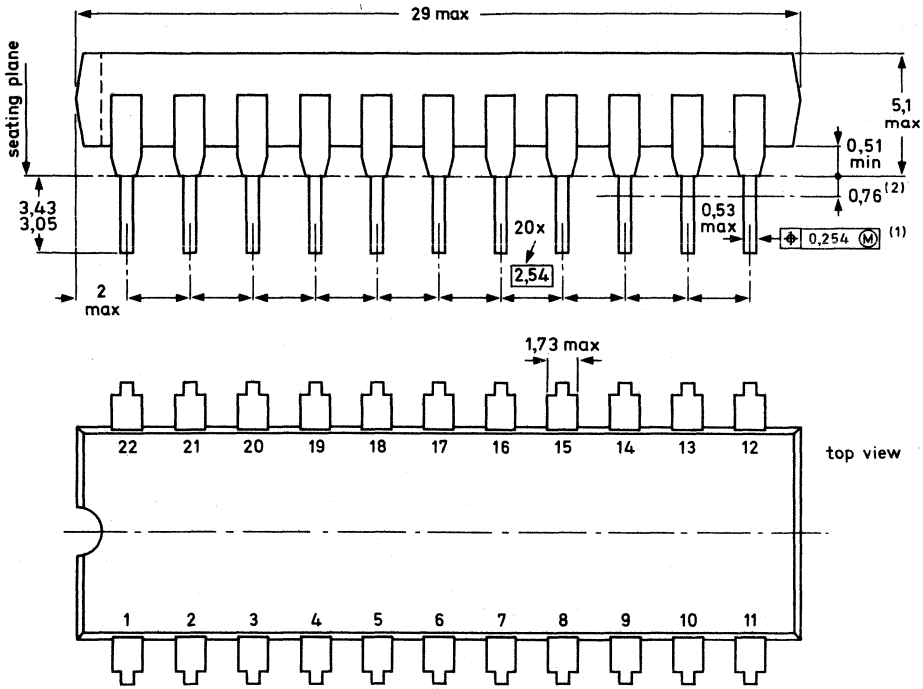
Ⓜ Maximum Material Condition.

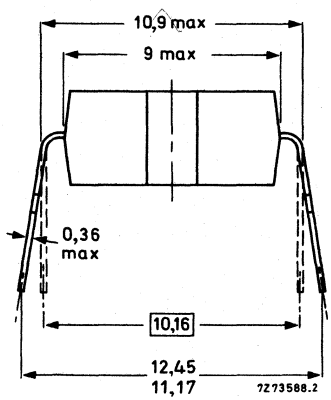
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

22-LEAD DUAL IN-LINE; PLASTIC (SOT-116)





side view

⊕ Positional accuracy.

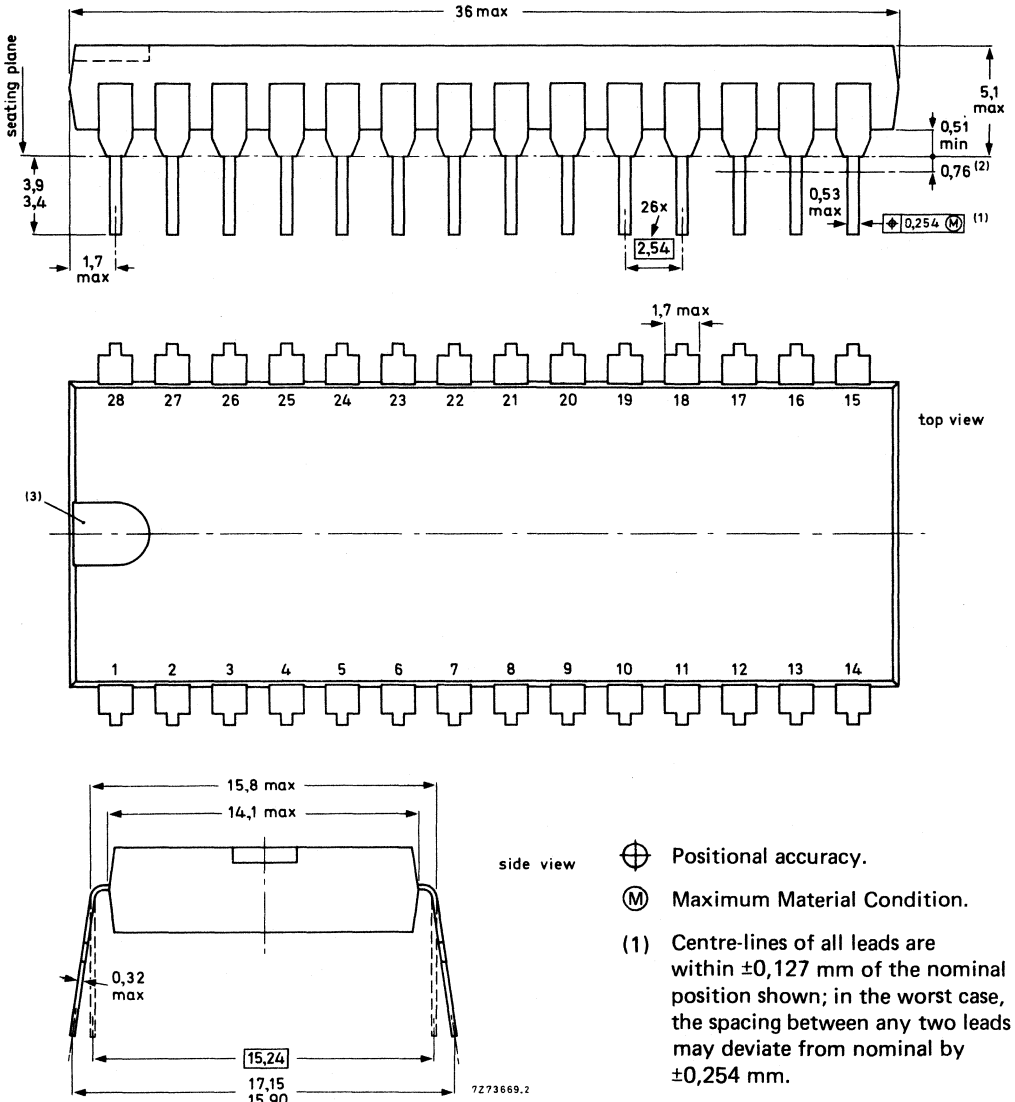
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

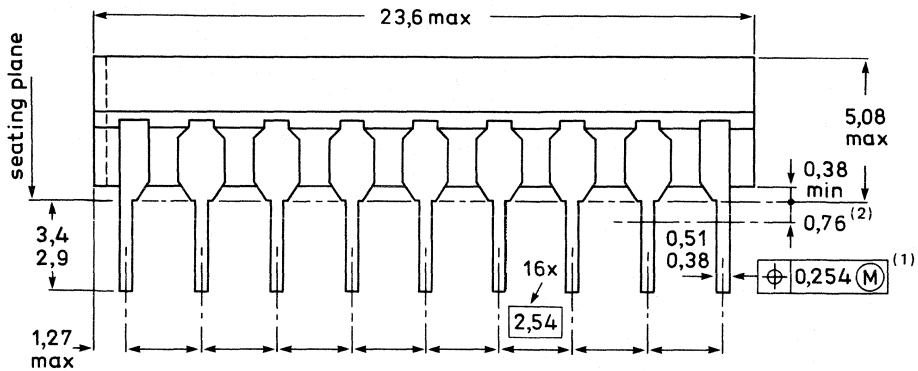
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

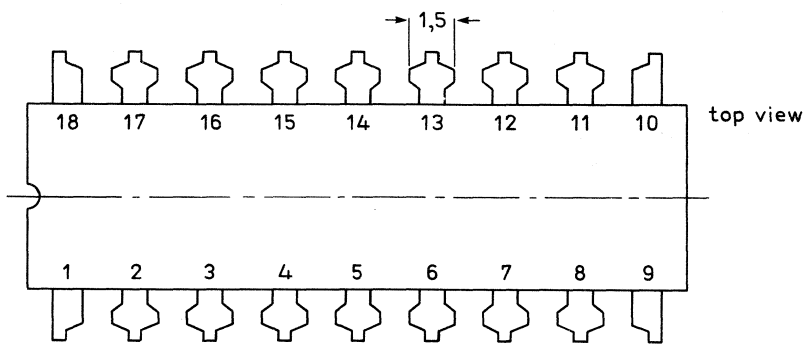
(2) Lead spacing tolerances apply from seating plane to the line indicated.

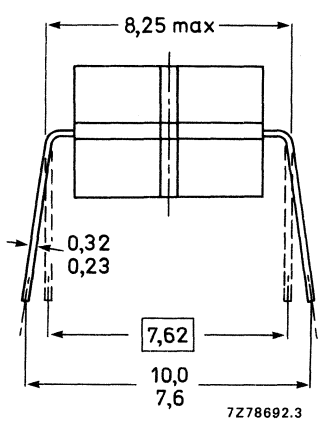
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133B)







⊕ Positional accuracy.

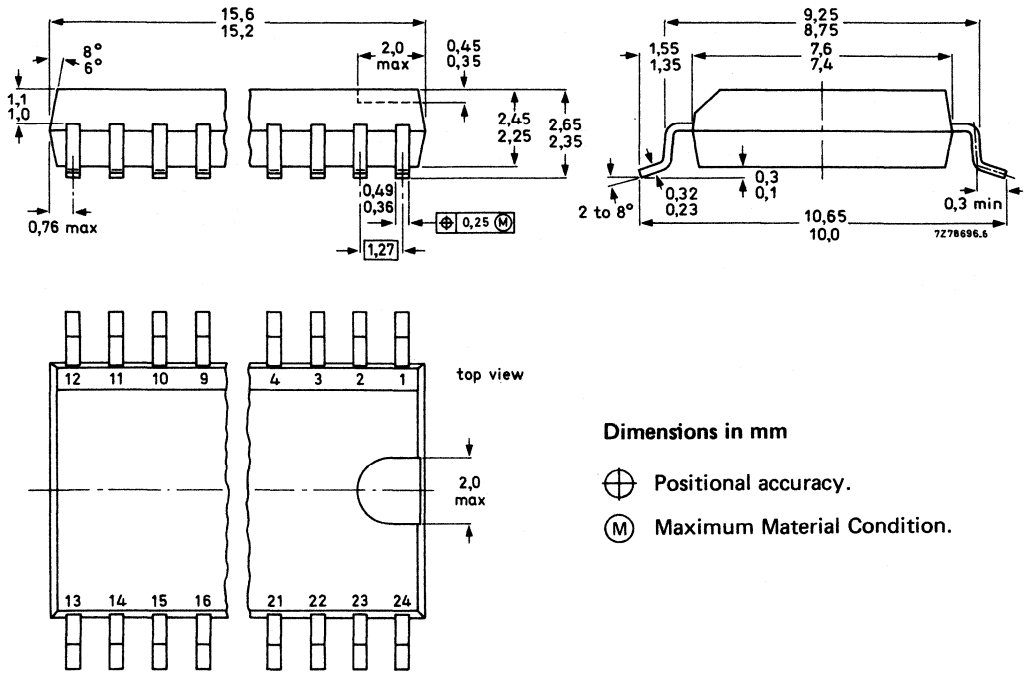
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)

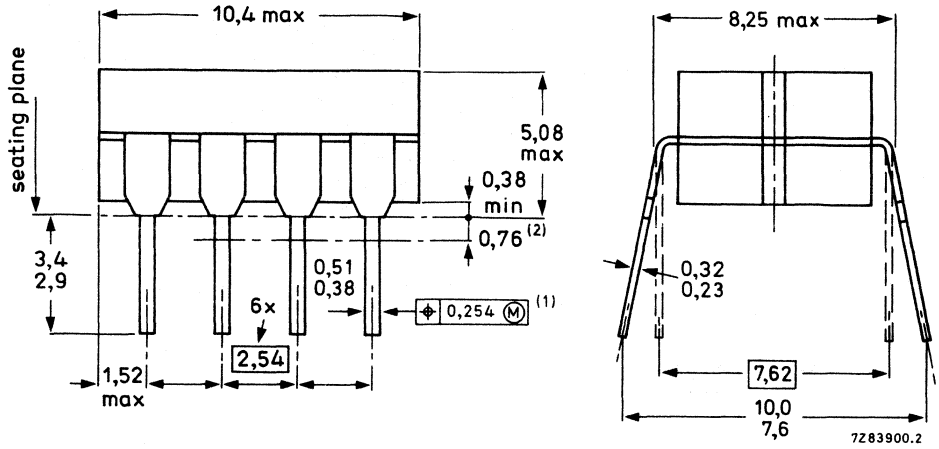


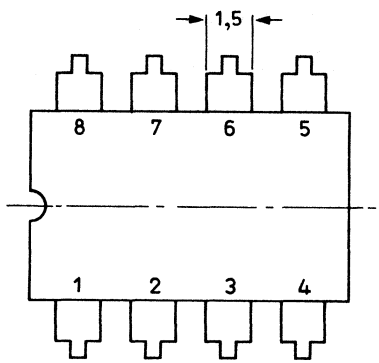
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

8-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-151A)





⊕ Positional accuracy.

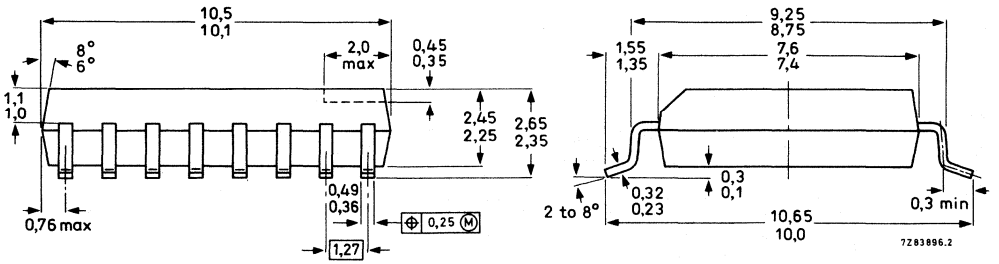
Ⓜ Maximum Material Condition.

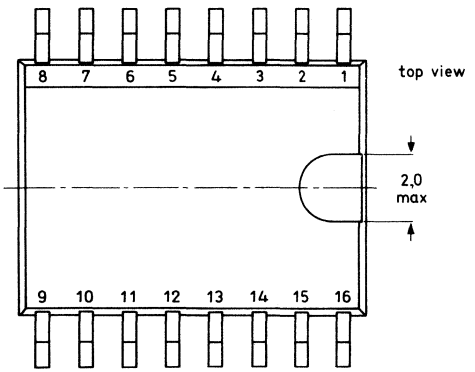
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)



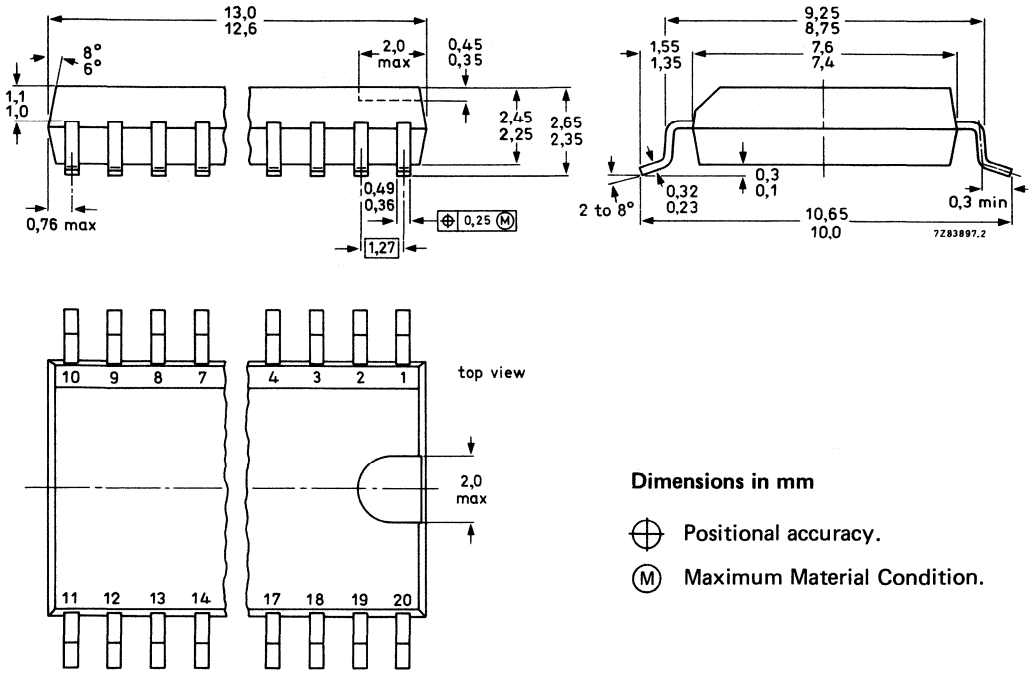


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)

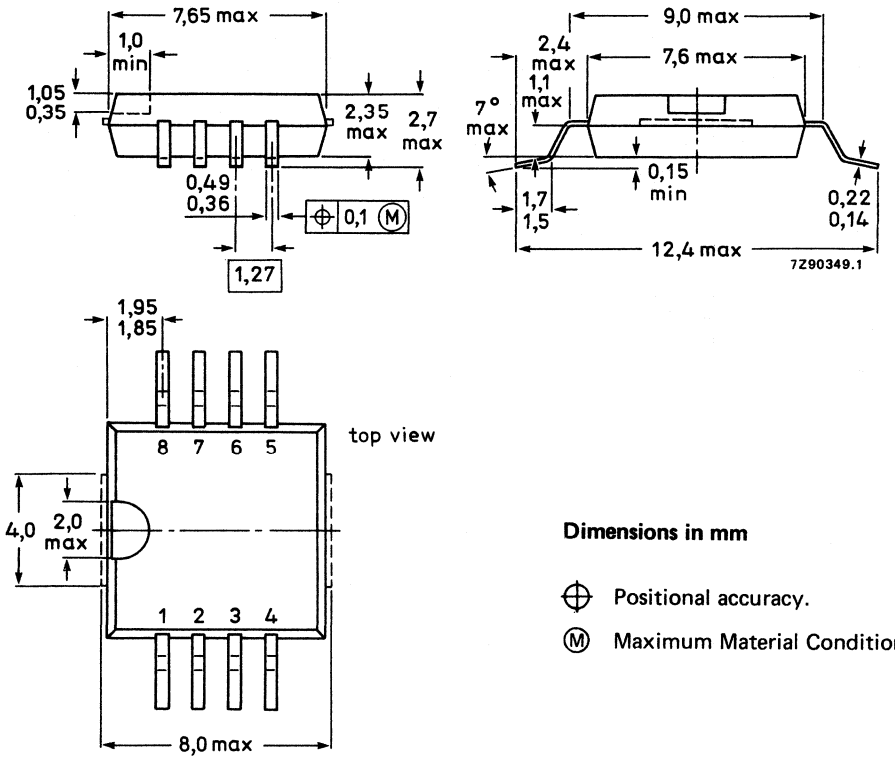


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

8-LEAD MINI-PACK; PLASTIC (SO-8L; SOT-176)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Soldering

SOLDERING PLASTIC DUAL IN-LINE (DIL) PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING PLASTIC MINI-PACK (SO) PACKAGES

1. By hand-held soldering iron or pulse-heated solder tool

Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A modified wave soldering technique is recommended, using two solder waves (dual-wave); a first turbulent wave with high upward pressure is followed by a smooth, laminar wave. A mildly activated flux will eliminate the need for removal of corrosive residues in most applications.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 8 and 60 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent, and to reduce thermal shock on entry to reflow zone.

4. Repairing soldered joints

The same precautions and limits apply as in (1) above.

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